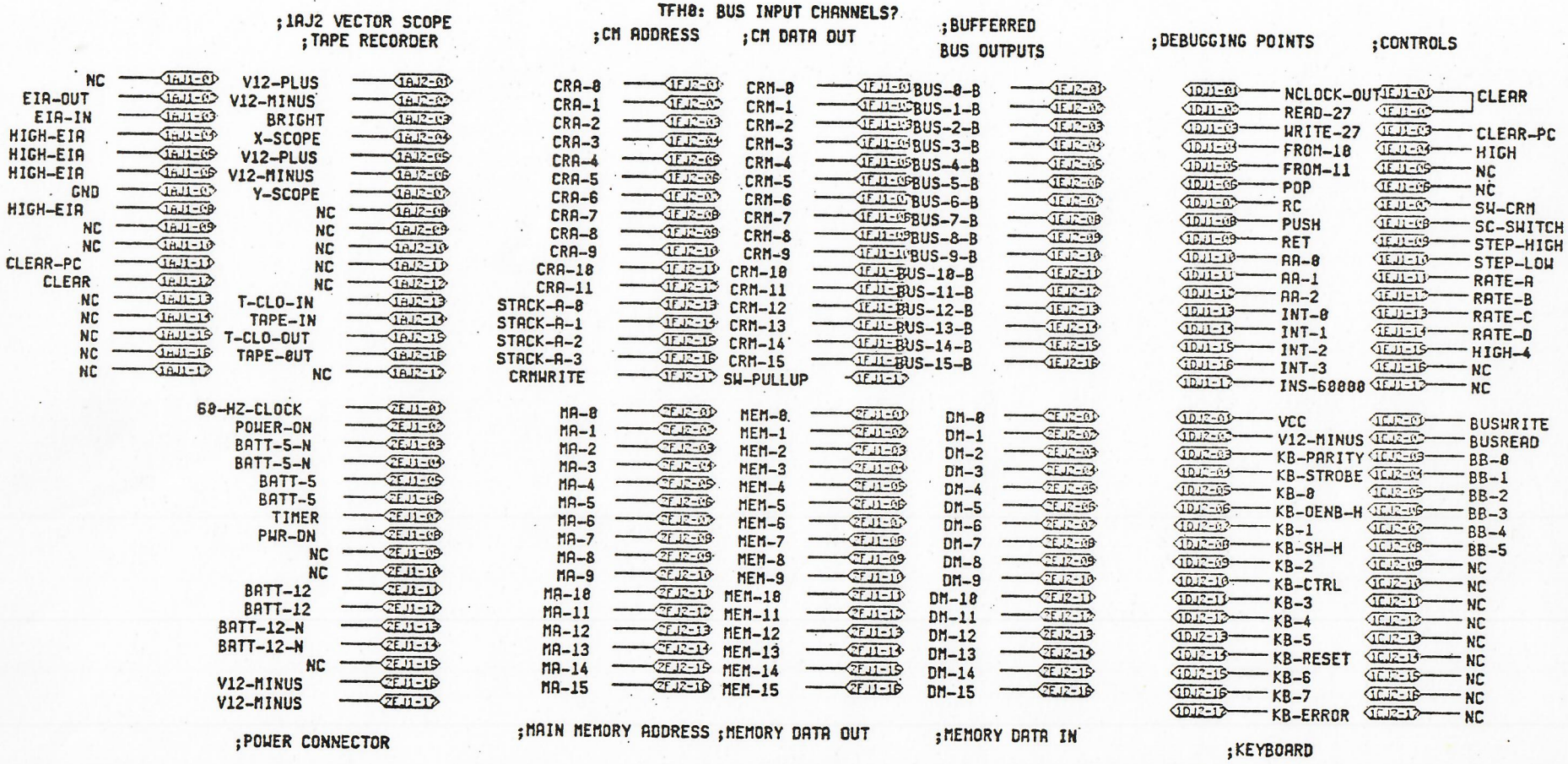
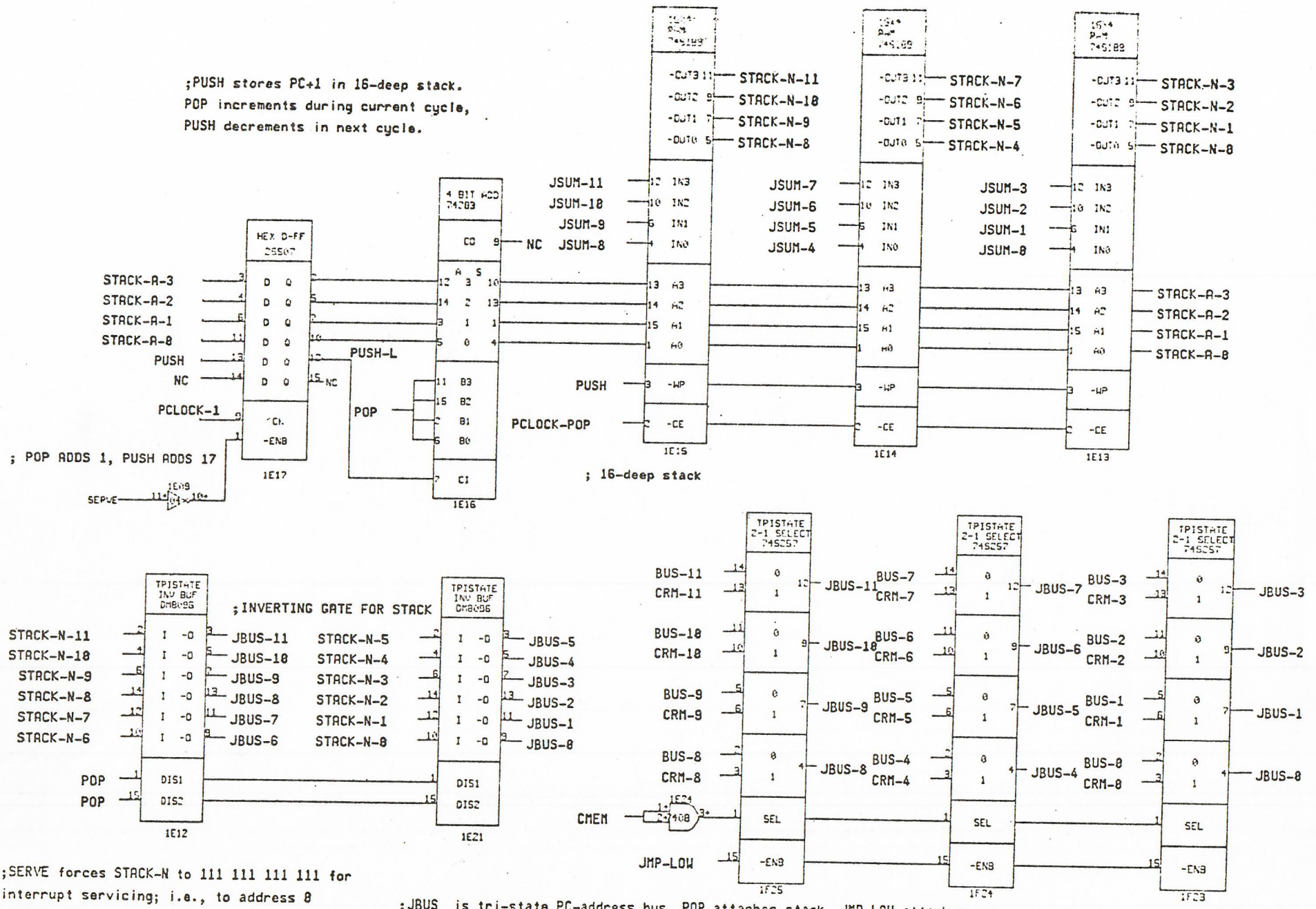
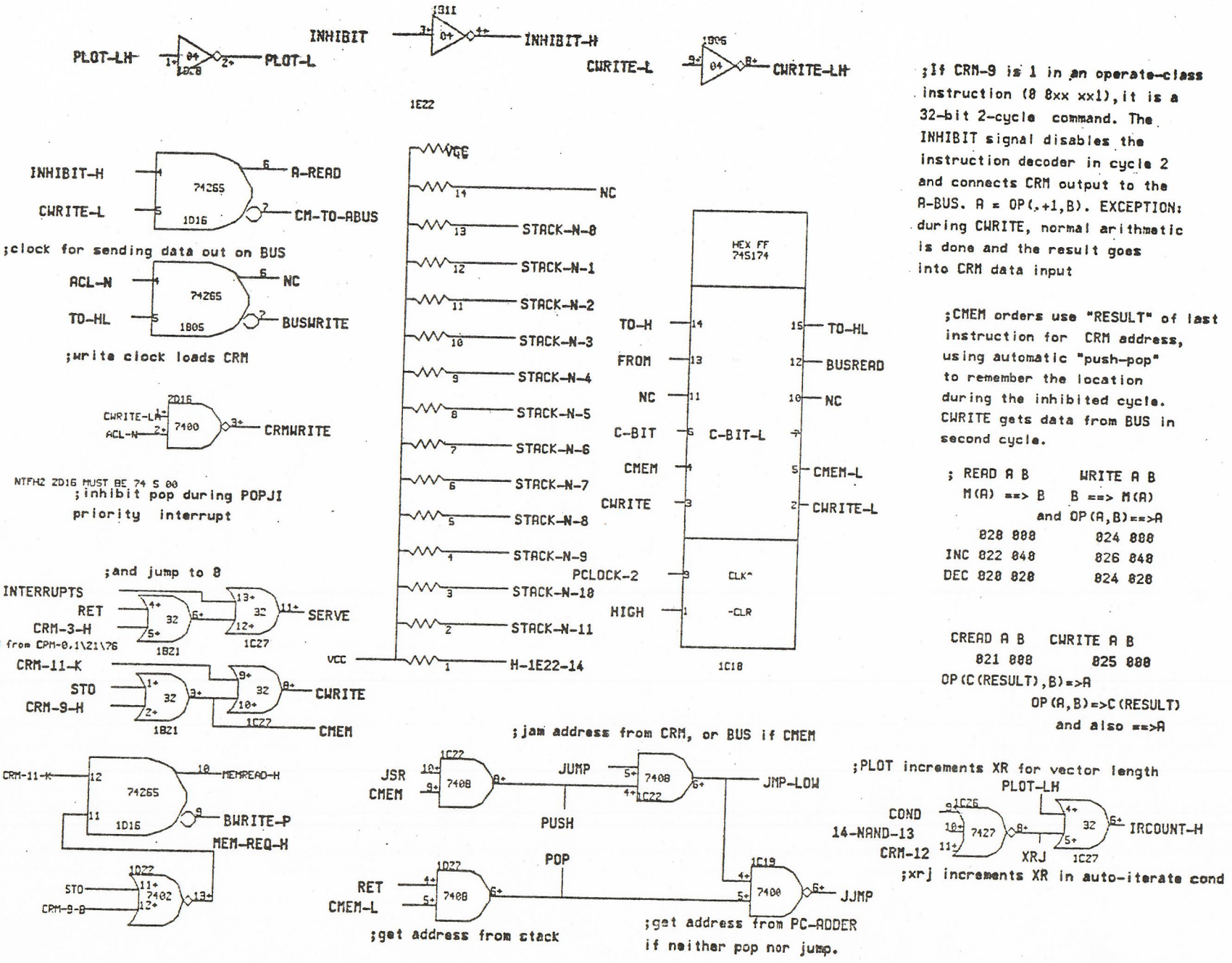
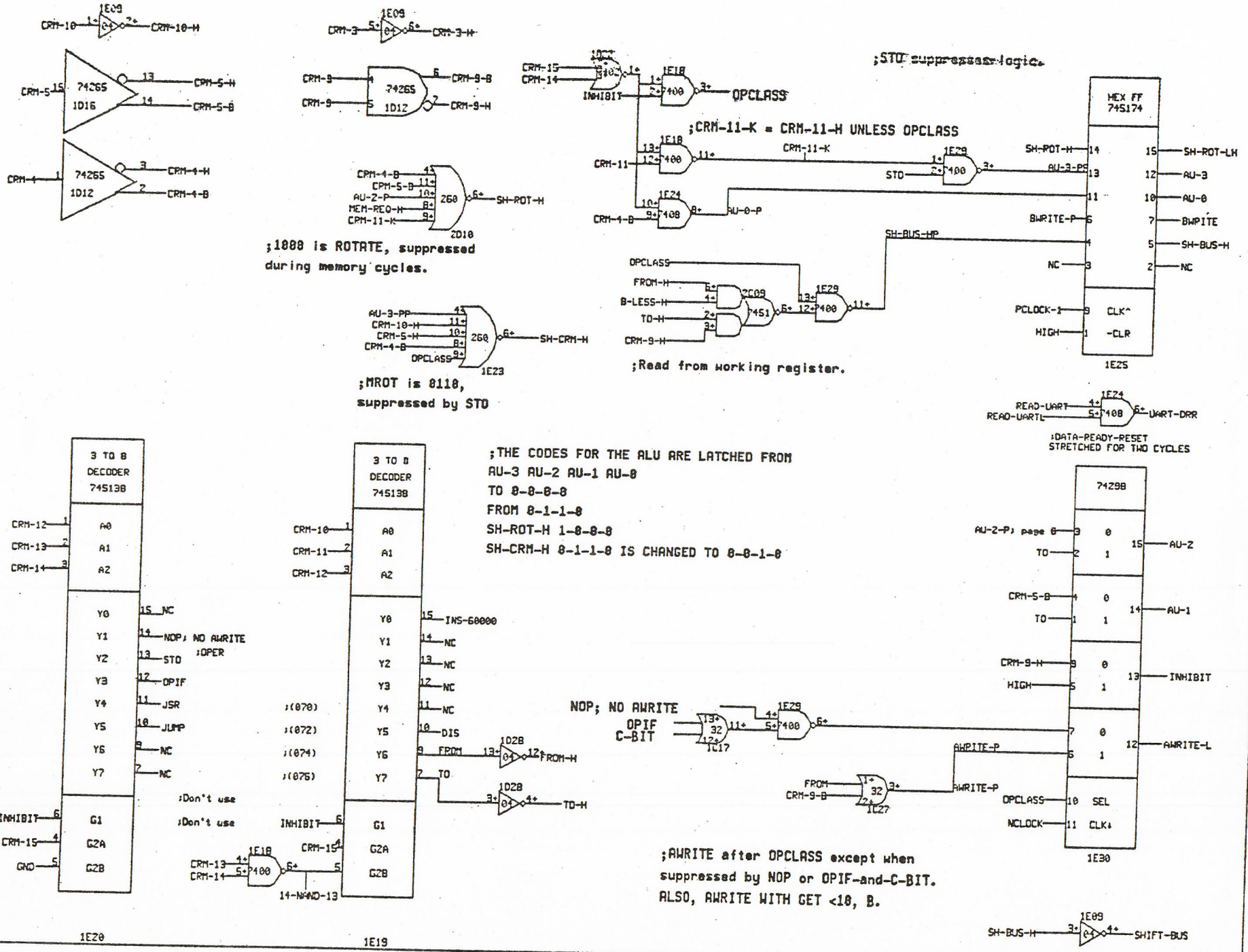
TFH8: BUS INPUT CHANNELS?



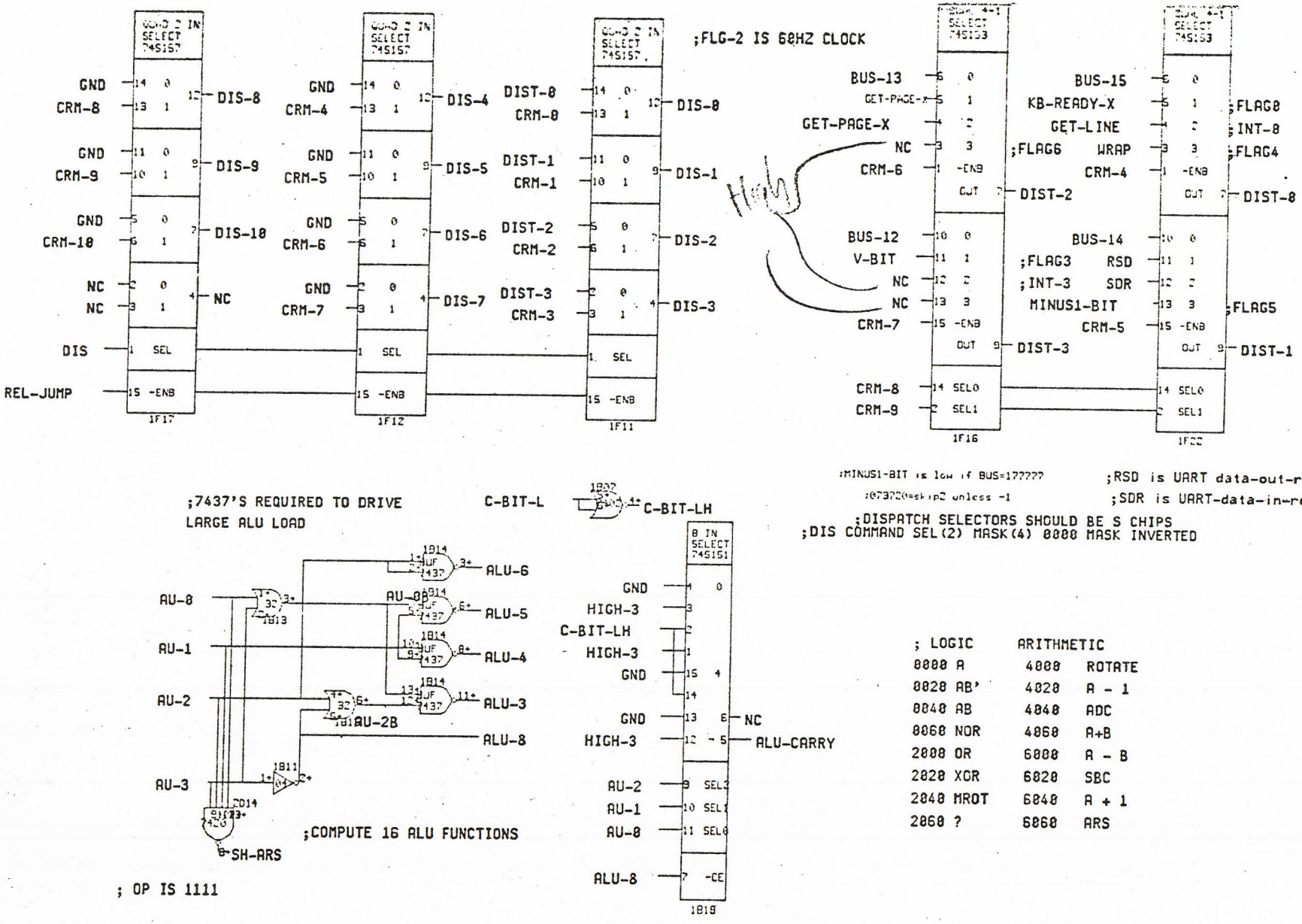


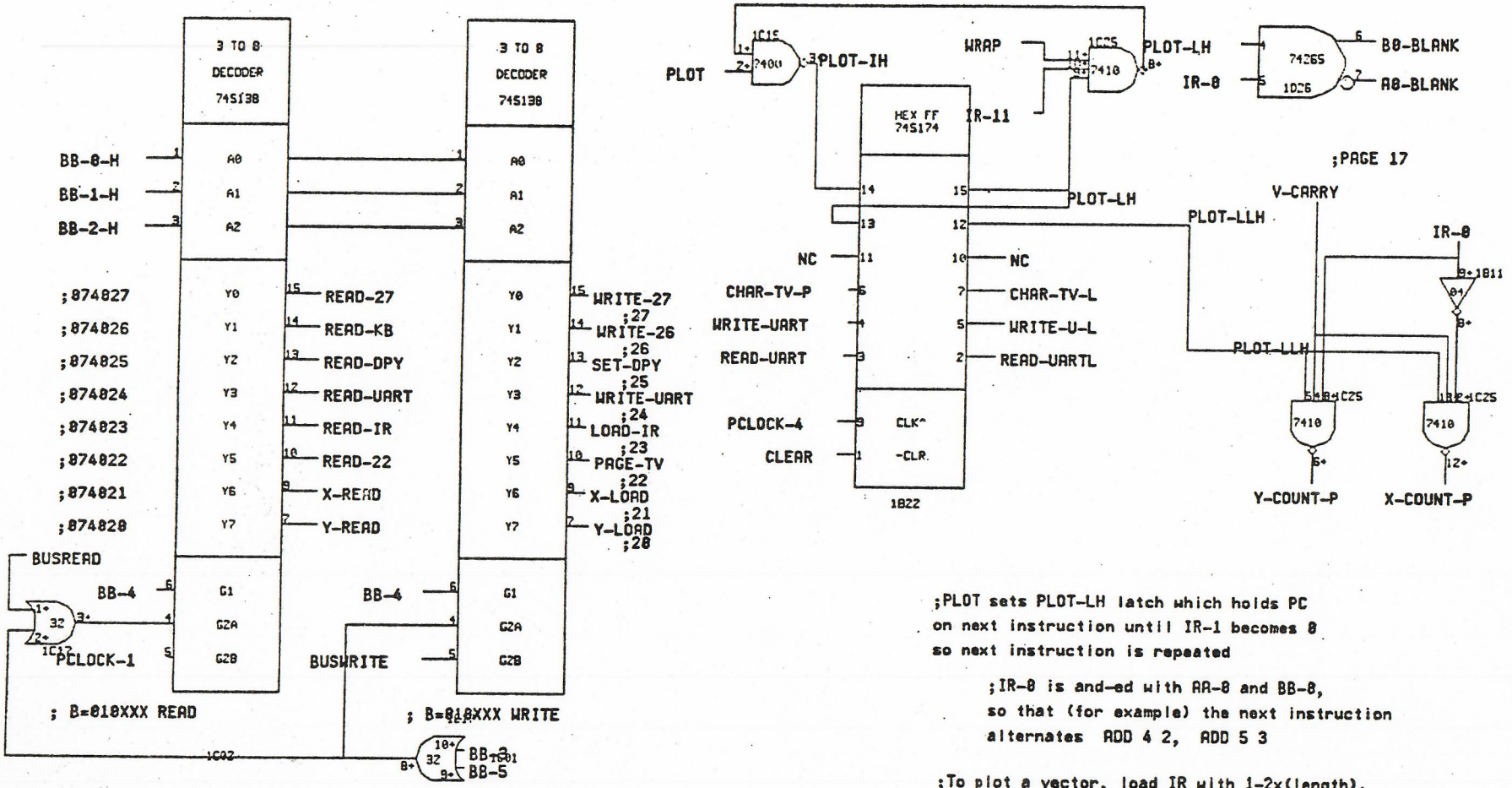
STACK TO PC GATE	STACK	05-APR-76 14:20	HQM: NTFH1


PLOT-LH
PLOT-L
INHIBIT
INHIBIT-H
CWRITE-L
CWRITE-LH
1E22
INHIBIT-H
CWRITE-L
74265
1D16
A-READ
CM-TO-ABUS
;clock for sending data out on BUS
ACL-N
TO-HL
74265
1B05
NC
BUSWRITE
;write clock loads CRM
2D16
CWRITE-LH
ACL-N
7400
CRMWRITE
NTFH2 2D16 MUST BE 74 S 00
;inhibit pop during POPJI
priority interrupt
;and jump to 8
INTERRUPTS
RET
CRM-3-H
;changed from CRM-0,1\21\76
1B21
1C27
SERVE
CRM-11-K
STO
CRM-9-H
1B21
1C22
CWRITE
CMEM
VCC
NC
STACK-N-0
STACK-N-1
STACK-N-2
STACK-N-3
STACK-N-4
STACK-N-5
STACK-N-6
STACK-N-7
STACK-N-8
STACK-N-9
STACK-N-10
STACK-N-11
H-1E22-14
HEX FF
74S174
TO-H
FROM
NC
C-BIT
CMEM
CWRITE
C-BIT-L
TO-HL
BUSREAD
NC
CMEM-L
CWRITE-L
PCLOCK-2
HIGH
CLK^
-CLR
1C18
;If CRM-9 is 1 in an operate-class instruction (8 8xx xx1), it is a 32-bit 2-cycle command. The INHIBIT signal disables the instruction decoder in cycle 2 and connects CRM output to the A-BUS. A = OP(,+1,B). EXCEPTION: during CWRITE, normal arithmetic is done and the result goes into CRM data input
;CMEM orders use "RESULT" of last instruction for CRM address, using automatic "push-pop" to remember the location during the inhibited cycle. CWRITE gets data from BUS in second cycle.
; READ A B WRITE A B
M(A) ==> B B ==> M(A)
and OP(A,B)==>A
828 888 824 888
INC 822 848 826 848
DEC 828 828 824 828
CREAD A B CWRITE A B
821 888 825 888
OP(C(RESULT),B)=>A
OP(A,B)=>C(RESULT)
and also ==>A
CRM-11-K
74265
1D16
MEMREAD-H
BWRITE-P
MEM-REQ-H
1D22
STO
CRM-9-B
7402
;jam address from CRM, or BUS if CMEM
JSR
CMEM
1C22
7408
JUMP
PUSH
JMP-LOW
RET
CMEM-L
1D27
POP
1C19
JJMP
;get address from stack
;get address from PC-ADDER if neither pop nor jump.
;PLOT increments XR for vector length
PLOT-LH
COND
14-NAND-13
CRM-12
1C26
7427
XRJ
32
1C27
IRCOUNT-H
;xrj increments XR in auto-iterate cond



INSTRUCTION DECODER	MINSKY 2500	29-FEB-76 13:07	HQM: NTFH3

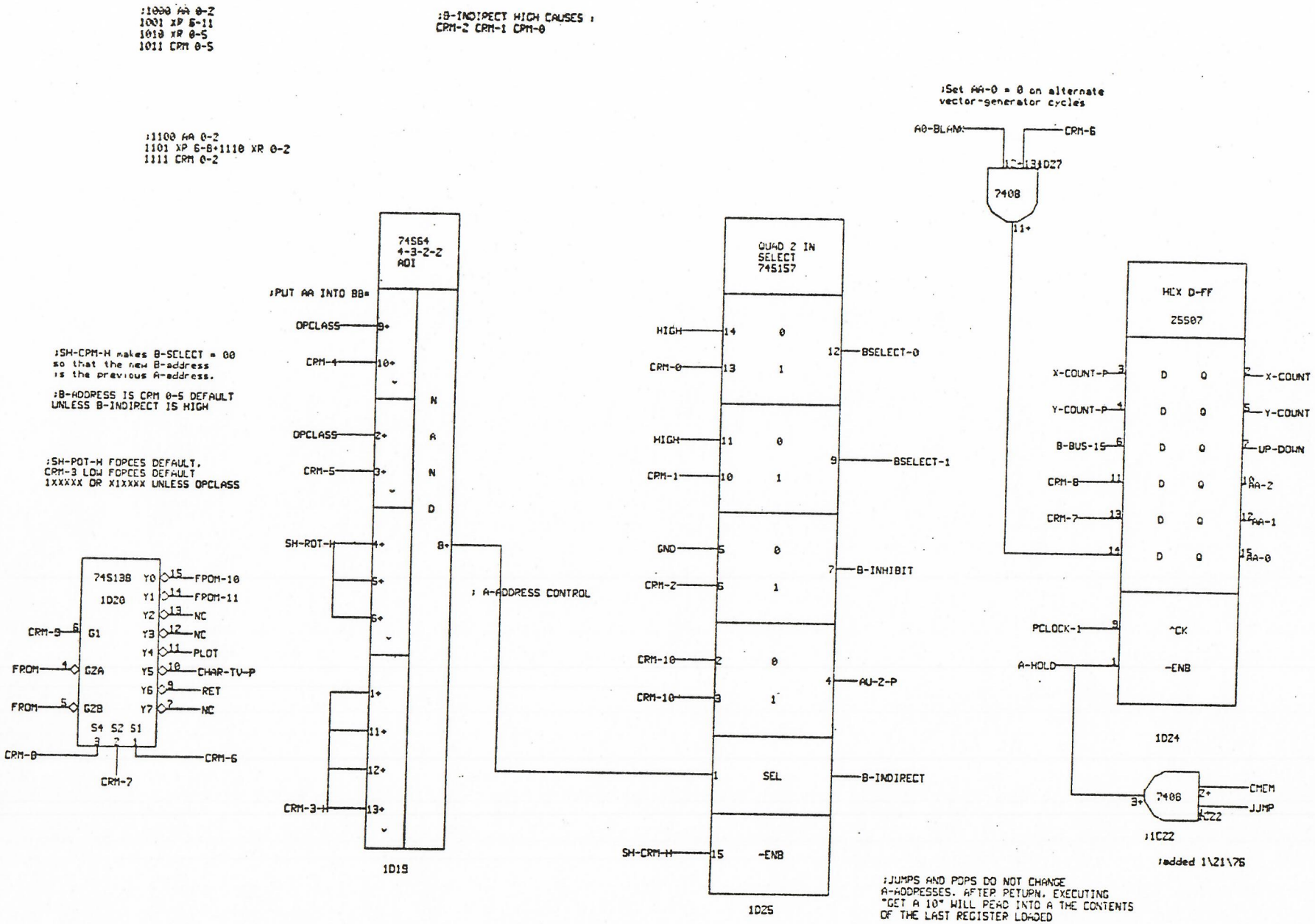

;FLG-2 IS 60HZ CLOCK
GND
CRM-8
DIS-8
GND
CRM-9
DIS-9
GND
CRM-10
DIS-10
NC
NC
NC
DIS
REL-JUMP
SEL
-ENB
1F17
GND
CRM-4
DIS-4
GND
CRM-5
DIS-5
GND
CRM-6
DIS-6
GND
CRM-7
DIS-7
1F12
DIST-0
CRM-0
DIS-0
DIST-1
CRM-1
DIS-1
DIST-2
CRM-2
DIS-2
DIST-3
CRM-3
DIS-3
1F11
BUS-13
GET-PAGE-X
NC
CRM-6
BUS-12
V-BIT
NC
NC
CRM-7
DIST-2
DIST-3
CRM-8
CRM-9
1F16
BUS-15
KB-READY-X
GET-LINE
;FLAG6
WRAP
CRM-4
BUS-14
;FLAG3
RSD
;INT-3
SDR
MINUS1-BIT
CRM-5
;FLAG0
;INT-8
;FLAG4
;FLAG5
DIST-8
DIST-1
1F22
;MINUS1-BIT is low if BUS=177777
;RSD is UART data-out-ready
;SDR is UART-data-in-ready
;DISPATCH SELECTORS SHOULD BE S CHIPS
;DIS COMMAND SEL(2) MASK(4) 0000 MASK INVERTED
;7437'S REQUIRED TO DRIVE
LARGE ALU LOAD
C-BIT-L
C-BIT-LH
AU-0
AU-1
AU-2
AU-3
ALU-6
ALU-5
ALU-4
ALU-3
ALU-8
AU-2B
SH-ARS
;COMPUTE 16 ALU FUNCTIONS
; OP IS 1111
GND
HIGH-3
C-BIT-LH
HIGH-3
GND
GND
HIGH-3
NC
ALU-CARRY
AU-2
AU-1
AU-0
ALU-8
-CE
1B19
;pin 6 inverts, diagram wrong!
; LOGIC ARITHMETIC
0000 A 4000 ROTATE
0020 AB' 4020 A - 1
0040 AB 4040 ADC
0060 NOR 4060 A+B
2000 OR 6000 A - B
2020 XOR 6020 SBC
2040 MROT 6040 A + 1
2060 ? 6060 ARS

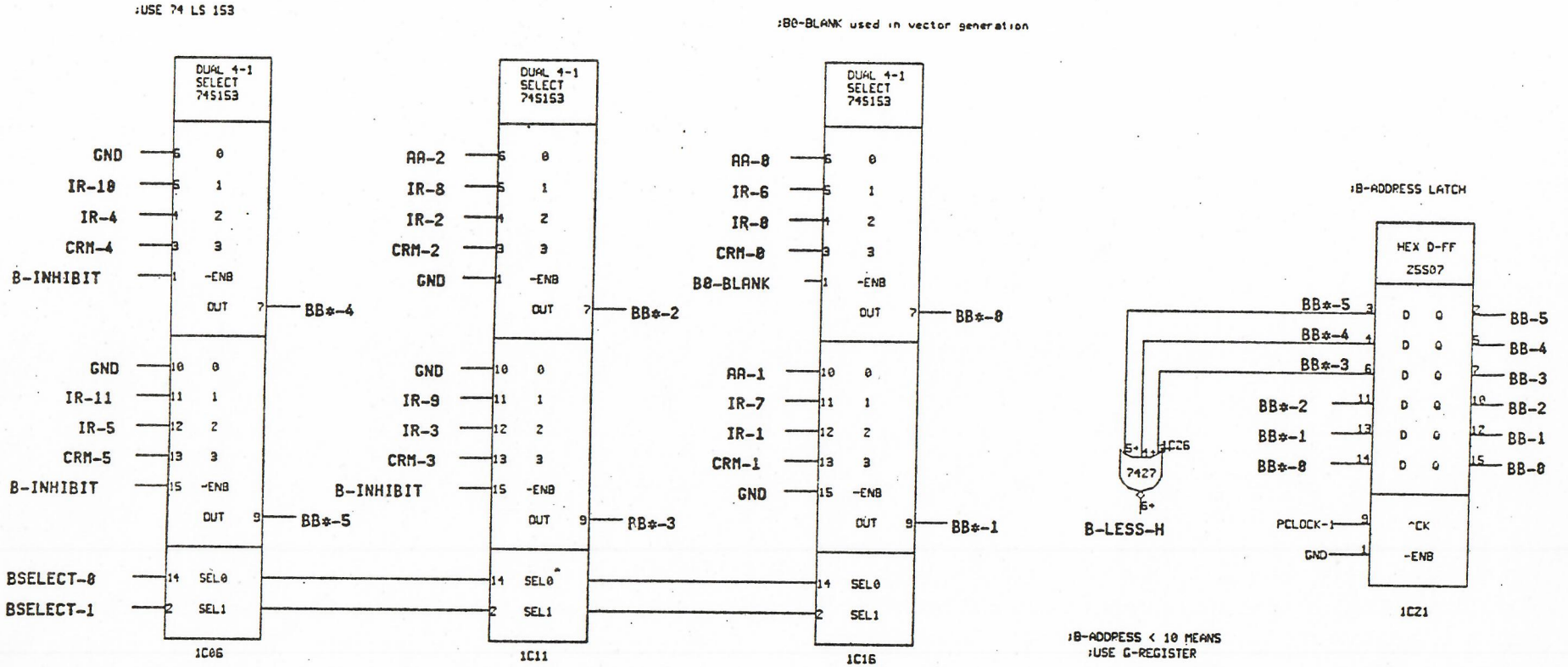


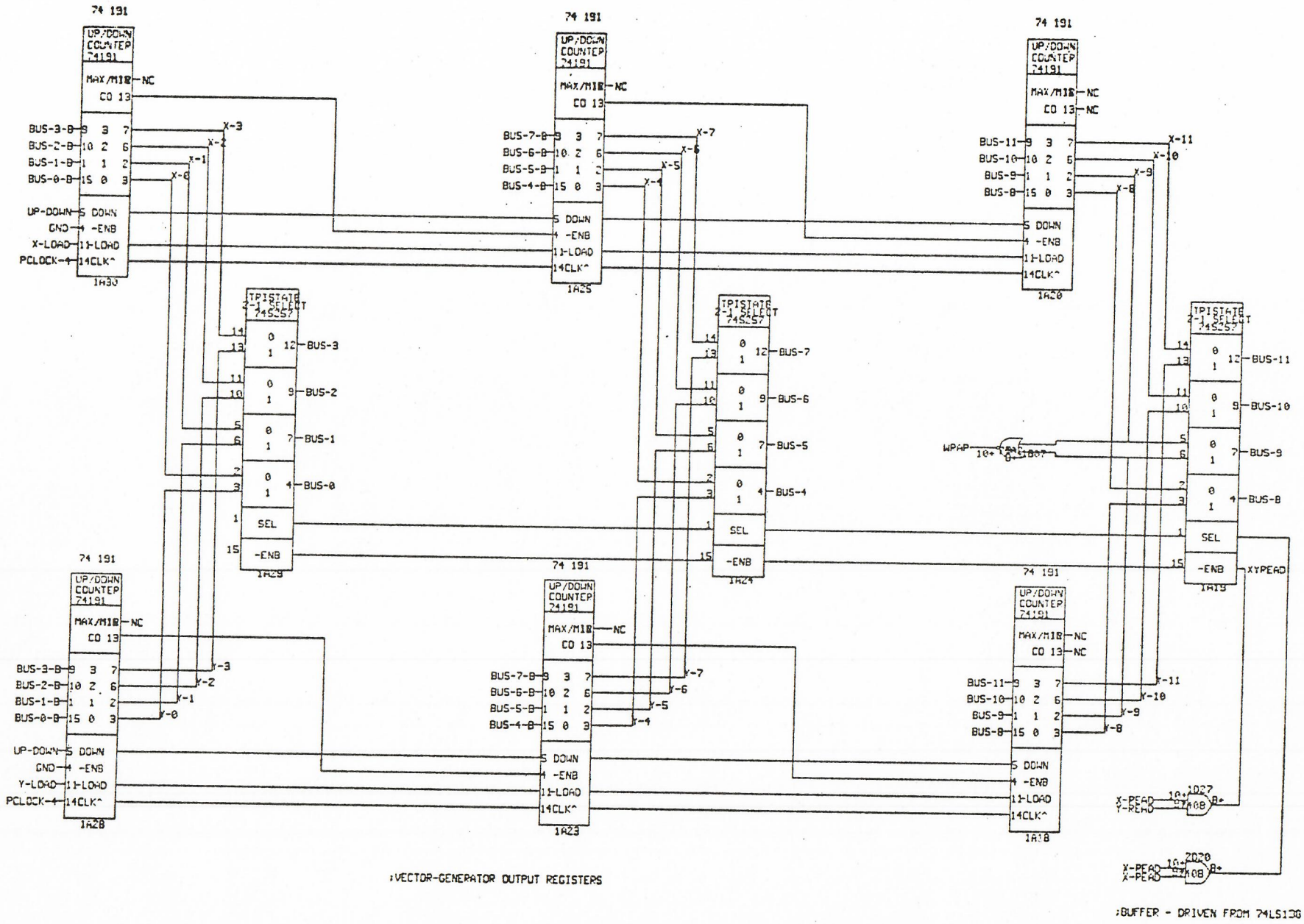
;PLOT sets PLOT-LH latch which holds PC on next instruction until IR-1 becomes 0 so next instruction is repeated

;IR-0 is and-ed with AA-0 and BB-0, so that (for example) the next instruction alternates ADD 4 2, ADD 5 3

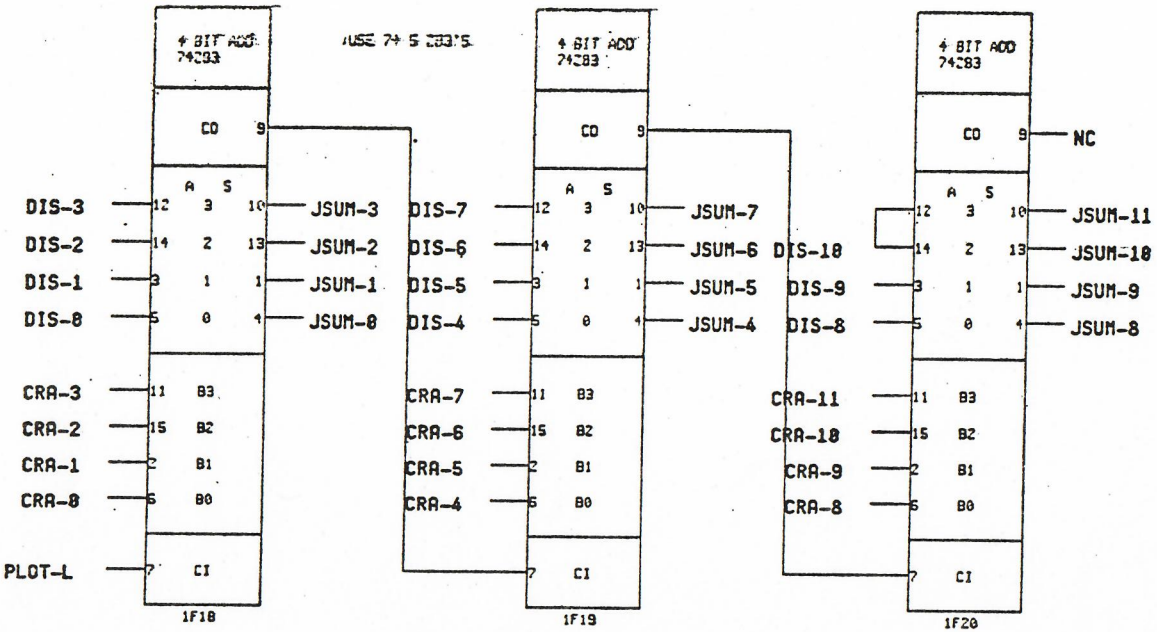
;To plot a vector, load IR with 1-2x(length). When an ADD overflows, the X or Y counter selected by IR-0 is incremented or decremented according to the sign of the B-addend.


;1000 AA 0-2
1001 XP 6-11
1010 XR 0-5
1011 CRM 0-5
;1100 AA 0-2
1101 XP 6-8+1110 XR 0-2
1111 CRM 0-2
;B-INDIRECT HIGH CAUSES :
CRM-2 CRM-1 CRM-0
;Set AA-0 = 0 on alternate vector-generator cycles
A0-BLANK
CRM-6
7408
1D27
;SH-CRM-H makes B-SELECT = 00 so that the new B-address is the previous A-address.
;B-ADDRESS IS CRM 0-5 DEFAULT UNLESS B-INDIRECT IS HIGH
;SH-POT-H FORCES DEFAULT, CRM-3 LOW FORCES DEFAULT 1XXXXX OR X1XXXX UNLESS OPCLASS
74S138
1D20
G1
G2A
G2B
S4 S2 S1
FPDM-10
FPDM-11
NC
NC
PLOT
CHAR-TV-P
RET
NC
FROM
FROM
CRM-8
CRM-7
CRM-6
74S64
4-3-2-2
AOI
;PUT AA INTO BB=
OPCLASS
CRM-4
OPCLASS
CRM-5
SH-ROT-H
CRM-3-H
NAND
1D19
; A-ADDRESS CONTROL
QUAD 2 IN SELECT 74S157
HIGH
CRM-0
HIGH
CRM-1
GND
CRM-2
CRM-10
CRM-10
SH-CRM-H
BSELECT-0
BSELECT-1
B-INHIBIT
AU-2-P
SEL
B-INDIRECT
-ENB
1D25
HEX D-FF
Z5507
X-COUNT-P
Y-COUNT-P
B-BUS-15
CRM-8
CRM-7
PCLOCK-1
A-HOLD
^CK
-ENB
X-COUNT
Y-COUNT
UP-DOWN
AA-2
AA-1
AA-0
1D24
7408
CMEM
JJMP
;1C22
;added 1\21\76
;JUMPS AND POPS DO NOT CHANGE A-ADDRESSES. AFTER RETURN, EXECUTING "GET A 10" WILL READ INTO A THE CONTENTS OF THE LAST REGISTER LOADED


;USE 74 LS 153
;B0-BLANK used in vector generation
DUAL 4-1 SELECT 74S153
GND
IR-10
IR-4
CRM-4
B-INHIBIT
BB*-4
GND
IR-11
IR-5
CRM-5
B-INHIBIT
BB*-5
BSELECT-0
BSELECT-1
1C06
AA-2
IR-8
IR-2
CRM-2
GND
BB*-2
GND
IR-9
IR-3
CRM-3
B-INHIBIT
RB*-3
1C11
AA-0
IR-6
IR-0
CRM-0
B0-BLANK
BB*-0
AA-1
IR-7
IR-1
CRM-1
GND
BB*-1
1C16
;B-ADDRESS LATCH
HEX D-FF
ZS507
BB*-5
BB*-4
BB*-3
BB*-2
BB*-1
BB*-0
BB-5
BB-4
BB-3
BB-2
BB-1
BB-0
7427
1C26
B-LESS-H
PCLOCK-1
GND
^CK
-ENB
1CZ1
;B-ADDRESS < 10 MEANS
;USE G-REGISTER
;IF B-ADDRESS IS SELECT FOR B-ADDRESS SOURCE
; 10 AA 0-2. This is forced by SH-CRM-H.
; 11 IR 6-11 or 6-8 if B-inhibit
; 12 IR 0-5 or 0-2 if B-inhibit
;CRM 0-5 DEFAULT



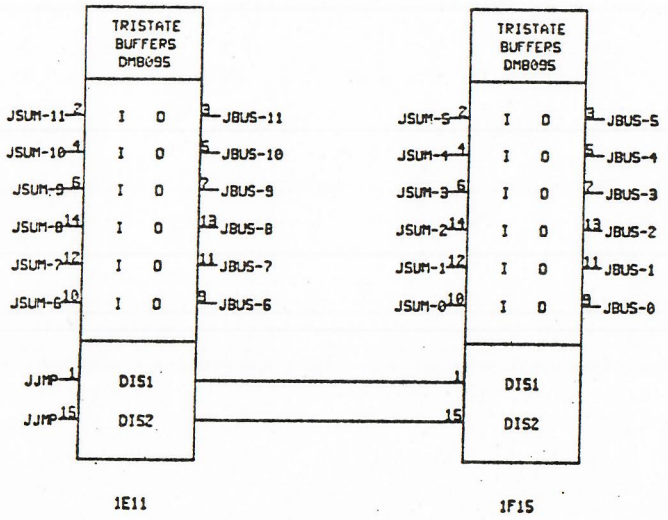
VECTOR GENERATOR	MINSKY 2500	02-APR-76 15:20	HQM: NTFH8



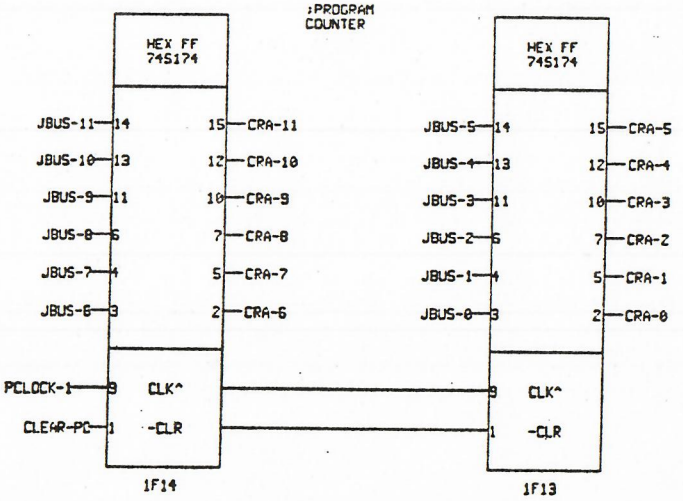
;BLOCKS ADD-1 DURING VECTOR

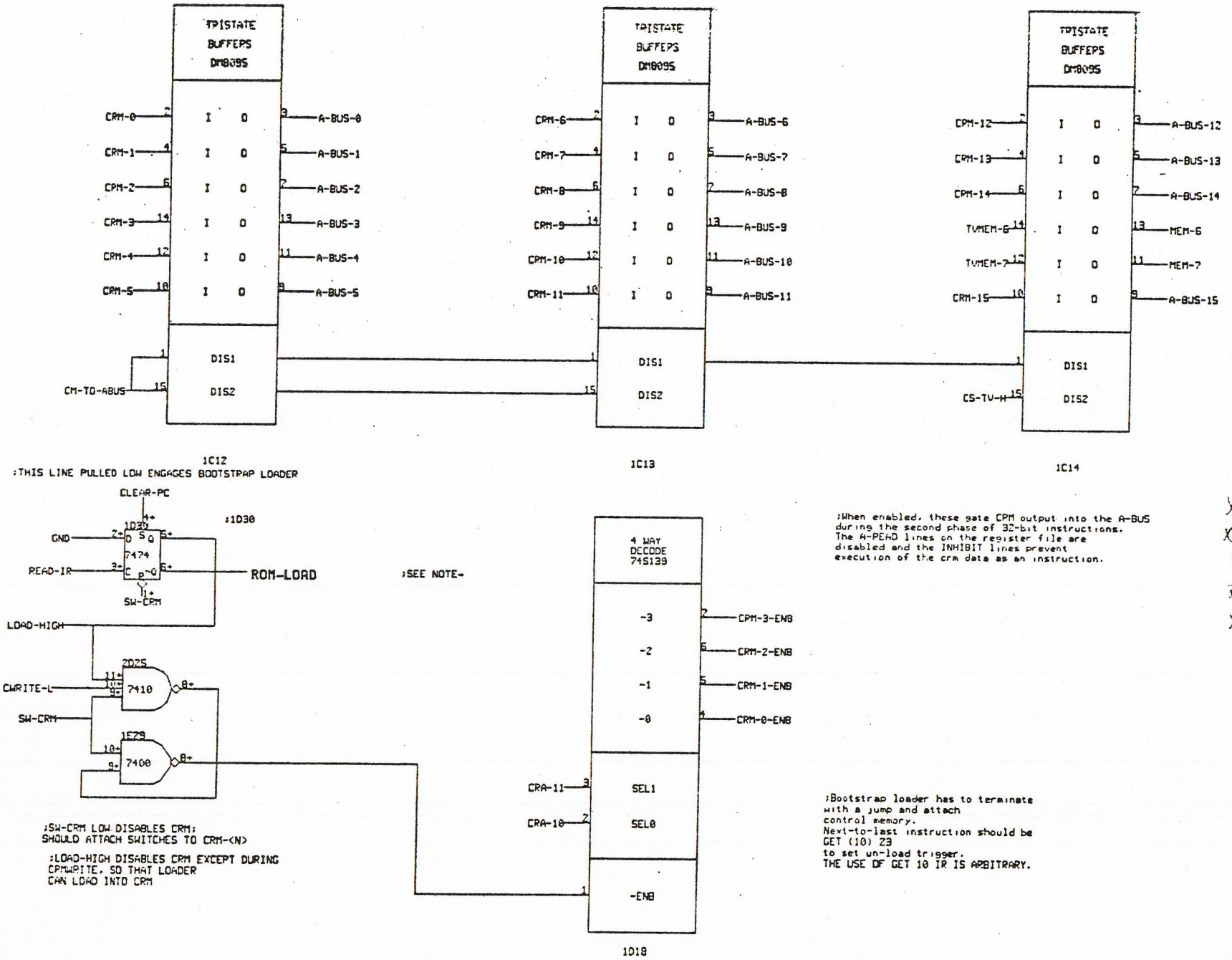
;12 BIT ADDER FOR INCREMENTING AND ADDING DISPATCH OFFSET

;USE 73 367'S

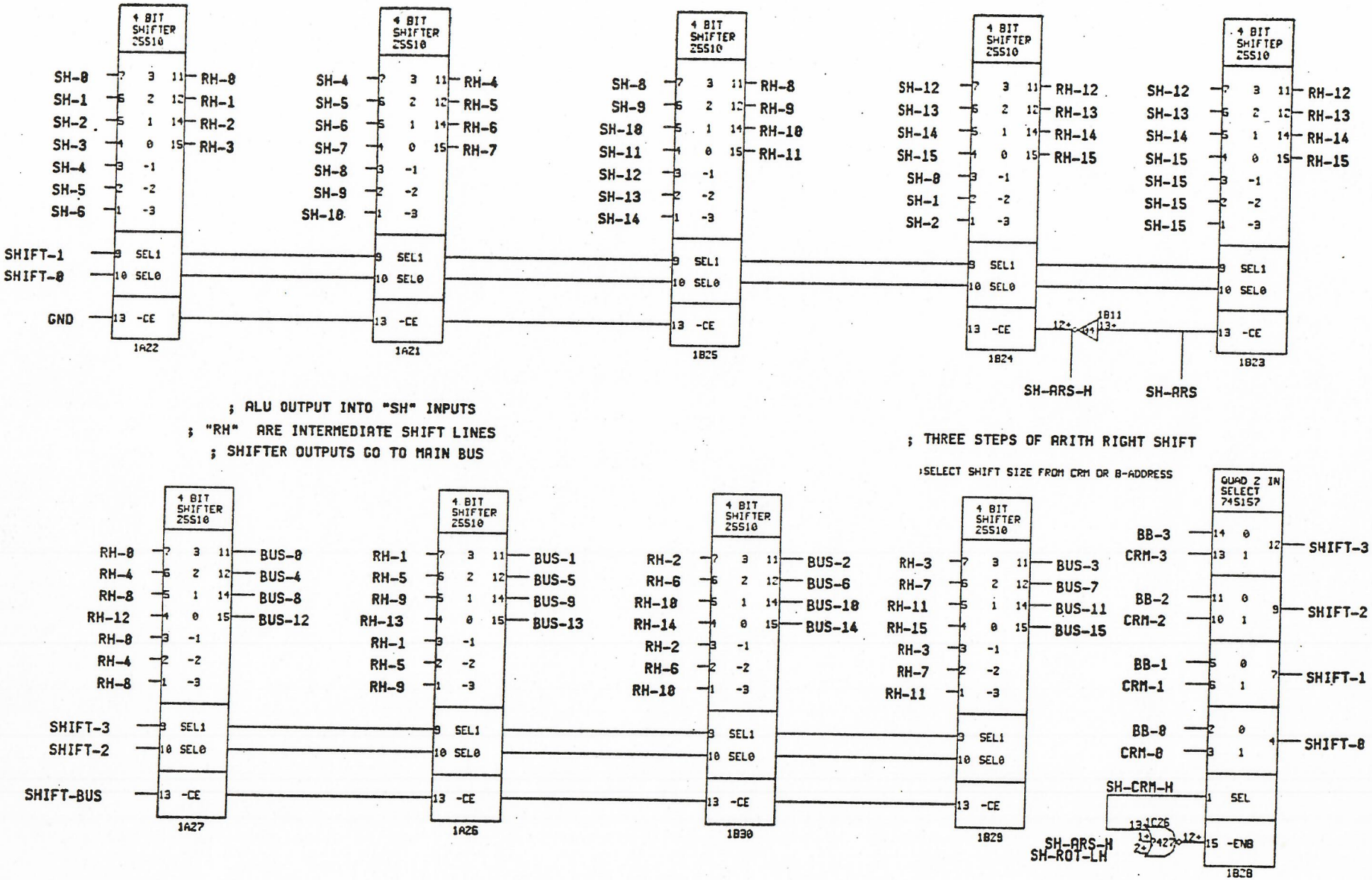


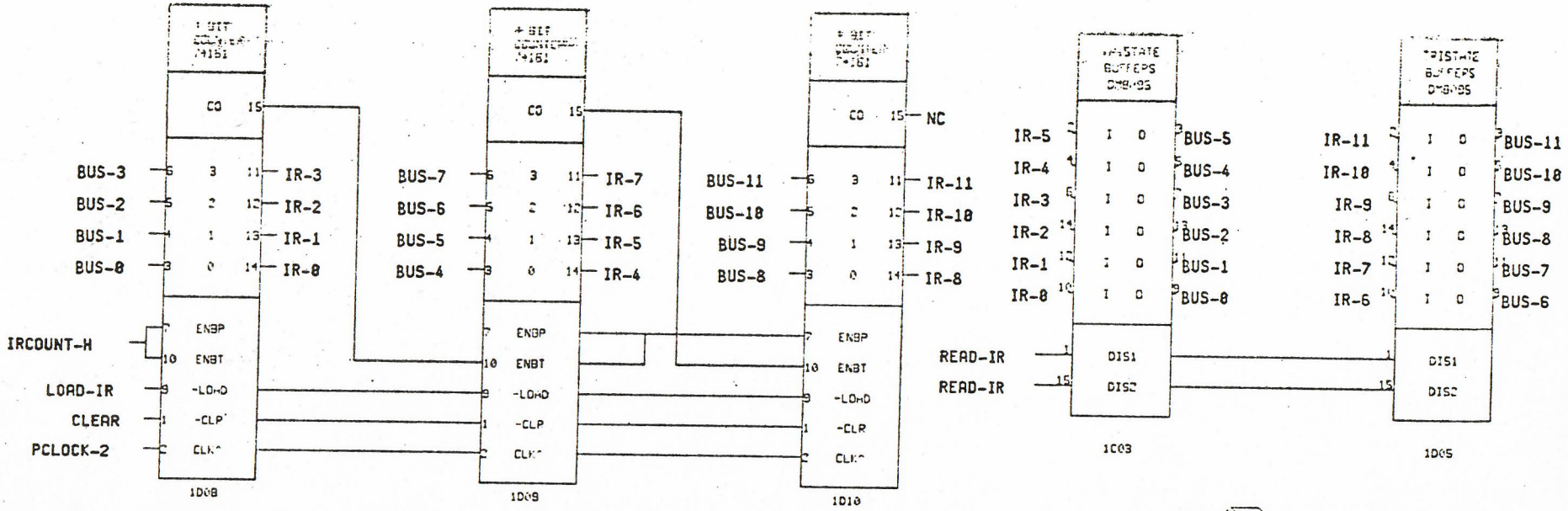
;PROGRAM COUNTER





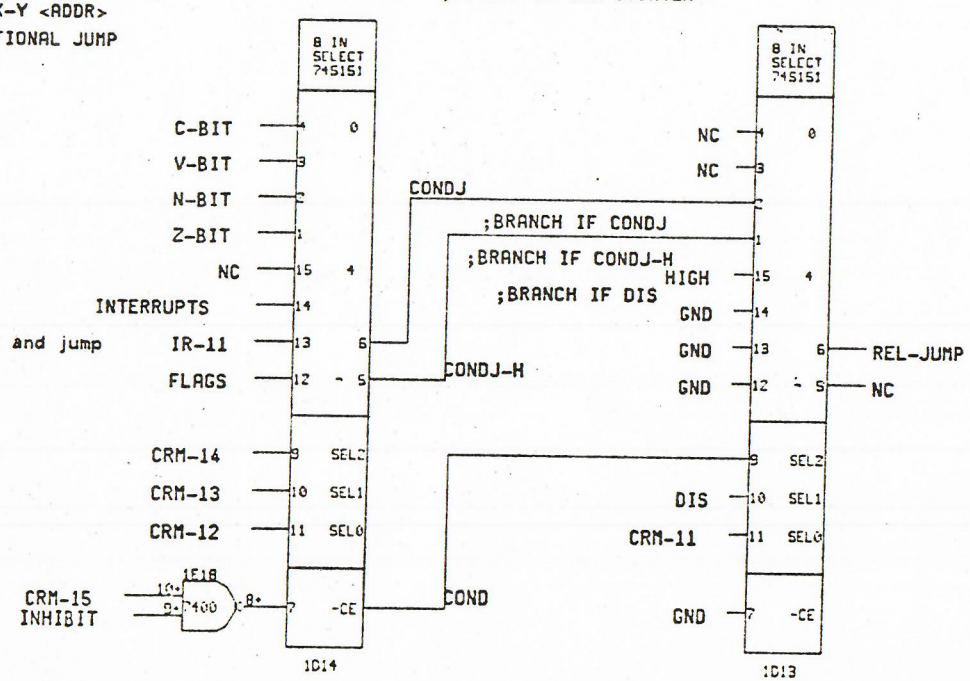
SHO
X1371
XSCA
13
DEFP
XTE


4 BIT SHIFTER 25S10
SH-0
SH-1
SH-2
SH-3
SH-4
SH-5
SH-6
RH-0
RH-1
RH-2
RH-3
SHIFT-1
SHIFT-0
GND
SEL1
SEL0
-CE
1A22
SH-4
SH-5
SH-6
SH-7
SH-8
SH-9
SH-10
RH-4
RH-5
RH-6
RH-7
1A21
SH-8
SH-9
SH-10
SH-11
SH-12
SH-13
SH-14
RH-8
RH-9
RH-10
RH-11
1B25
SH-12
SH-13
SH-14
SH-15
SH-8
SH-1
SH-2
RH-12
RH-13
RH-14
RH-15
1B24
1B11
SH-ARS-H
SH-ARS
1B23
; ALU OUTPUT INTO "SH" INPUTS
; "RH" ARE INTERMEDIATE SHIFT LINES
; SHIFTER OUTPUTS GO TO MAIN BUS
; THREE STEPS OF ARITH RIGHT SHIFT
;SELECT SHIFT SIZE FROM CRM OR B-ADDRESS
RH-0
RH-4
RH-8
RH-12
RH-1
RH-5
RH-9
RH-13
RH-2
RH-6
RH-10
RH-14
RH-3
RH-7
RH-11
RH-15
BUS-0
BUS-4
BUS-8
BUS-12
BUS-1
BUS-5
BUS-9
BUS-13
BUS-2
BUS-6
BUS-10
BUS-14
BUS-3
BUS-7
BUS-11
BUS-15
SHIFT-3
SHIFT-2
SHIFT-BUS
1A27
1A26
1B30
1B29
QUAD 2 IN SELECT 74S157
BB-3
CRM-3
BB-2
CRM-2
BB-1
CRM-1
BB-0
CRM-0
SHIFT-3
SHIFT-2
SHIFT-1
SHIFT-0
SH-CRM-H
SH-ARS-H
SH-ROT-LH
1C26
1B28

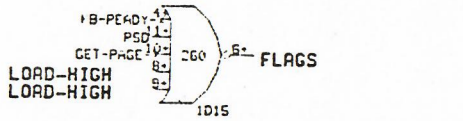


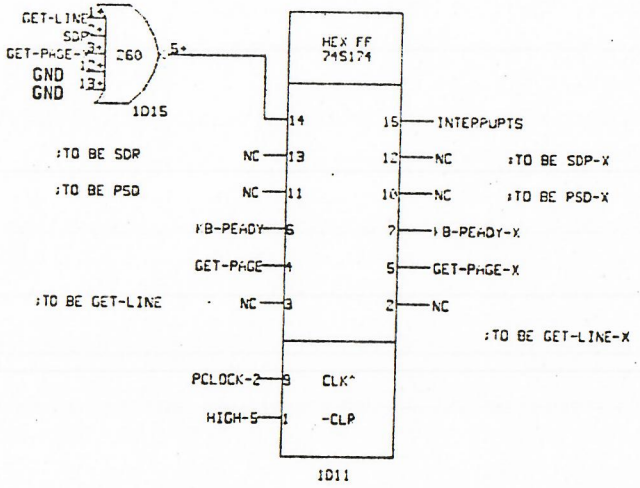
;12-BIT IR AND COUNTER

; 1-X-X-X-Y <ADDR>
IS CONDITIONAL JUMP

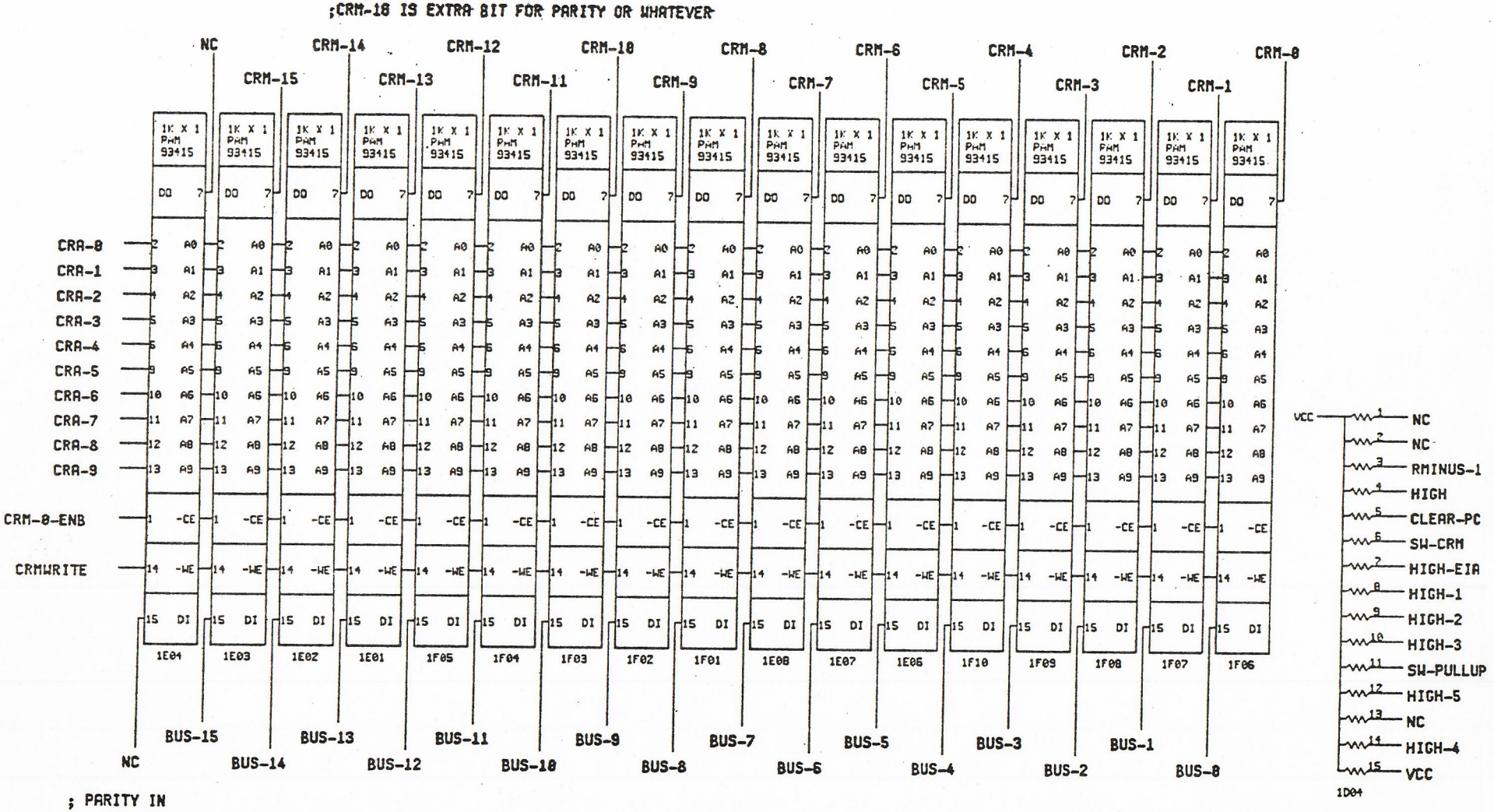


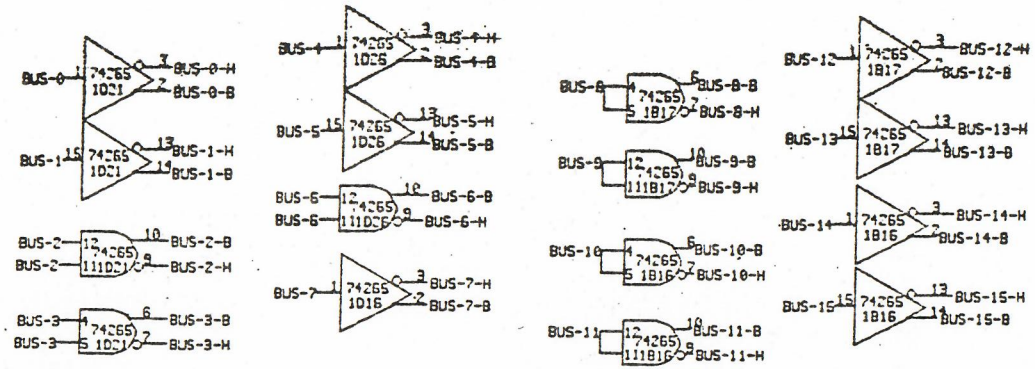
;Incr. IR and jump



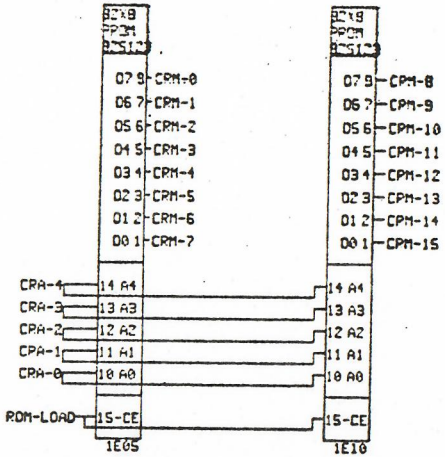


;LOAD-HIGH to make BPL branch
during ROM-LOAD

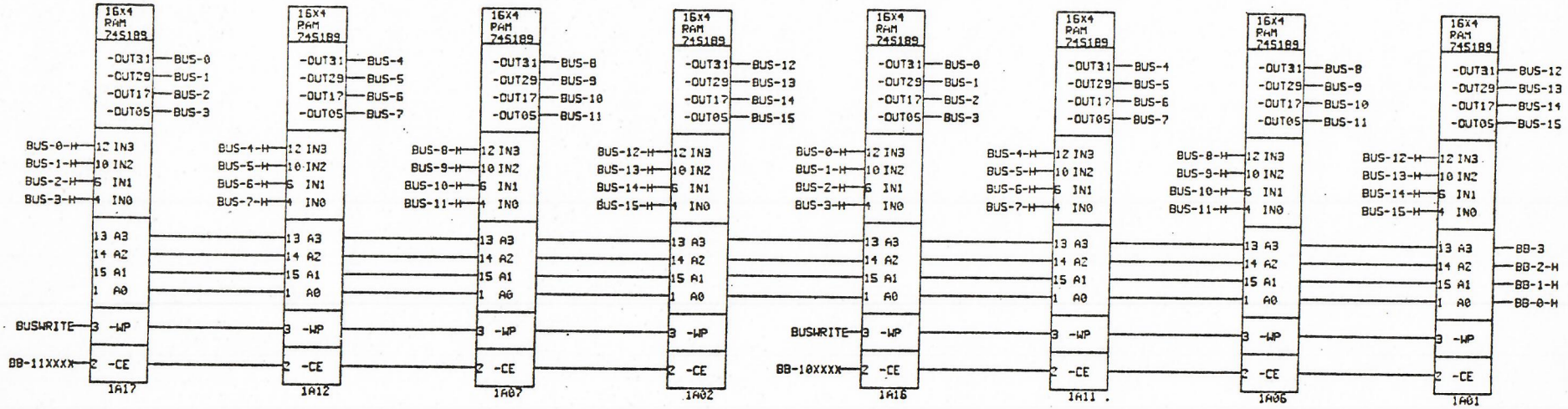

;CRM-18 IS EXTRA BIT FOR PARITY OR WHATEVER
NC
CRM-14
CRM-12
CRM-10
CRM-8
CRM-6
CRM-4
CRM-2
CRM-0
CRM-15
CRM-13
CRM-11
CRM-9
CRM-7
CRM-5
CRM-3
CRM-1
1K X 1 PHM 93415
DO 7
CRA-0
CRA-1
CRA-2
CRA-3
CRA-4
CRA-5
CRA-6
CRA-7
CRA-8
CRA-9
CRM-0-ENB
CRMWRITE
1E04
1E03
1E02
1E01
1F05
1F04
1F03
1F02
1F01
1E08
1E07
1E06
1F10
1F09
1F08
1F07
1F06
BUS-15
BUS-14
BUS-13
BUS-12
BUS-11
BUS-10
BUS-9
BUS-8
BUS-7
BUS-6
BUS-5
BUS-4
BUS-3
BUS-2
BUS-1
BUS-0
NC
; PARITY IN
VCC
NC
NC
RMINUS-1
HIGH
CLEAR-PC
SW-CRM
HIGH-EIA
HIGH-1
HIGH-2
HIGH-3
SW-PULLUP
HIGH-5
NC
HIGH-4
VCC
1D04
;14-PIN PULLUP
;USE 93425 TRI-STATE RAMS

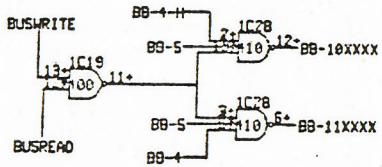


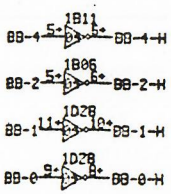
;BUS BUFFERRED FOR GENERAL OUTPUT USE

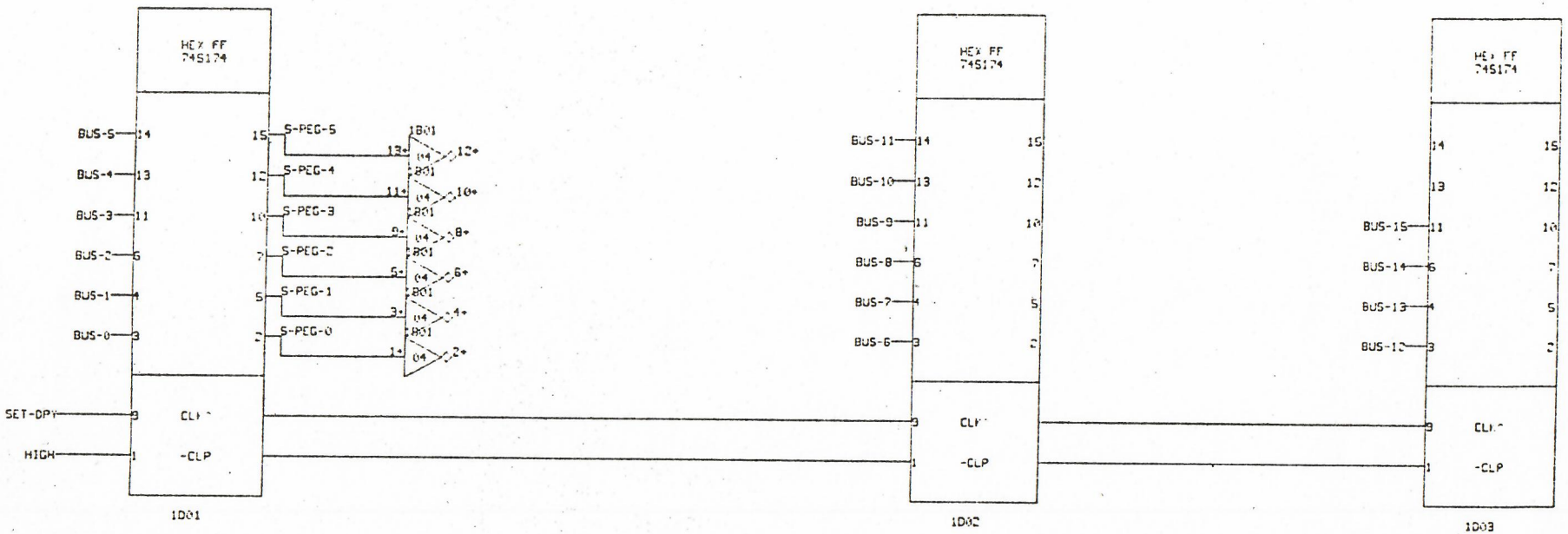


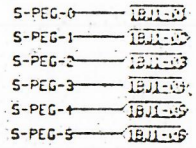
;SOCKETS FOR TWO 32 X 8
ROMS FOR LOADER



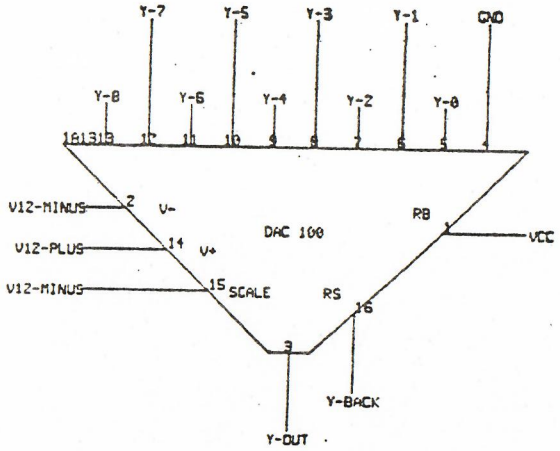






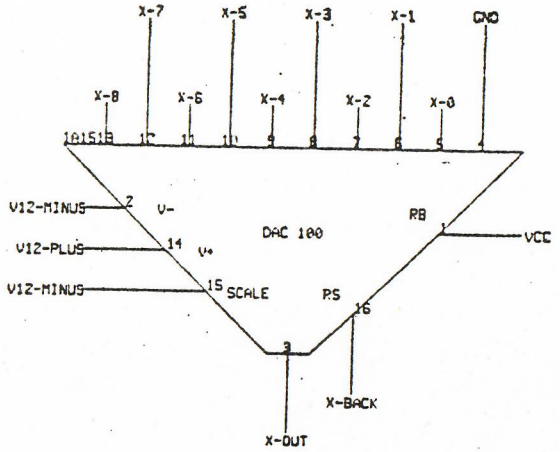


NOTES	TFH ORDER CODE	Ø4-APR-76 16:56	HQM: NTFH15



;1A15

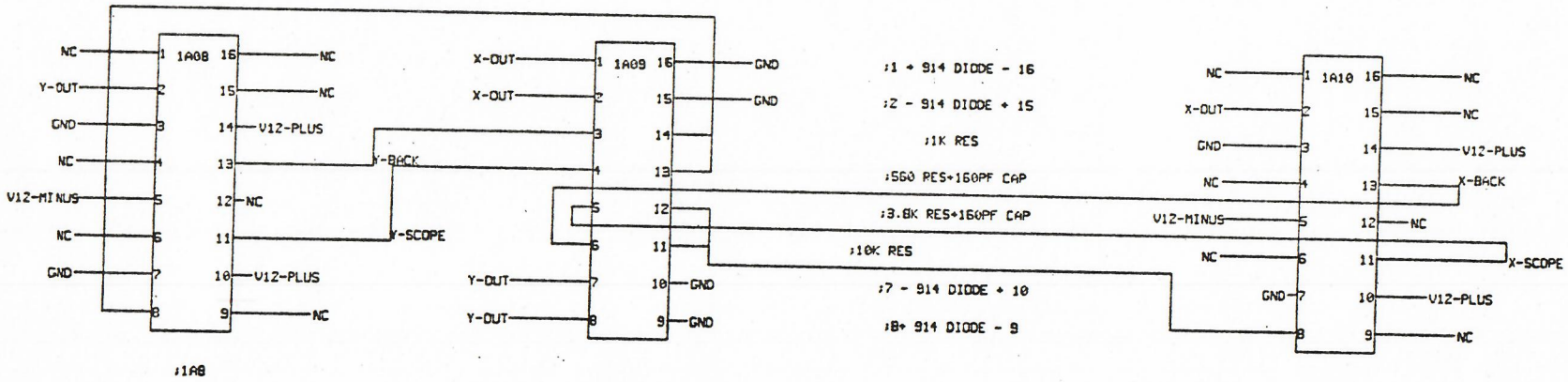
;1A13



; Y-OUT AND X-OUT NEED PROTECTION DIODES

;1A9

; THIS IS A 72747 OP-AMP



;1A8

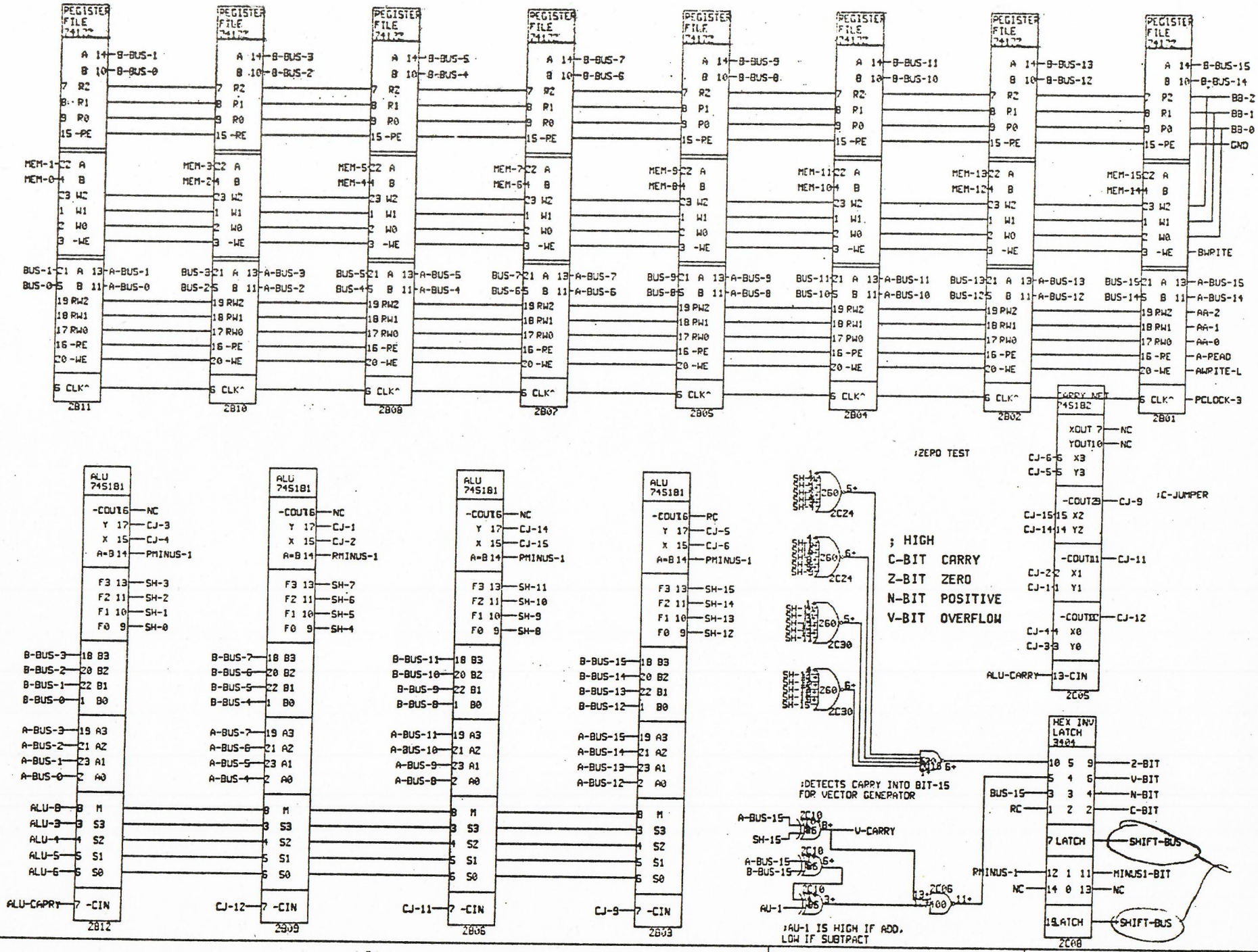
; ANALOG FEEDBACK NET

;PINS 4 AND 10 EACH HAVE 470PF CAP TO GND

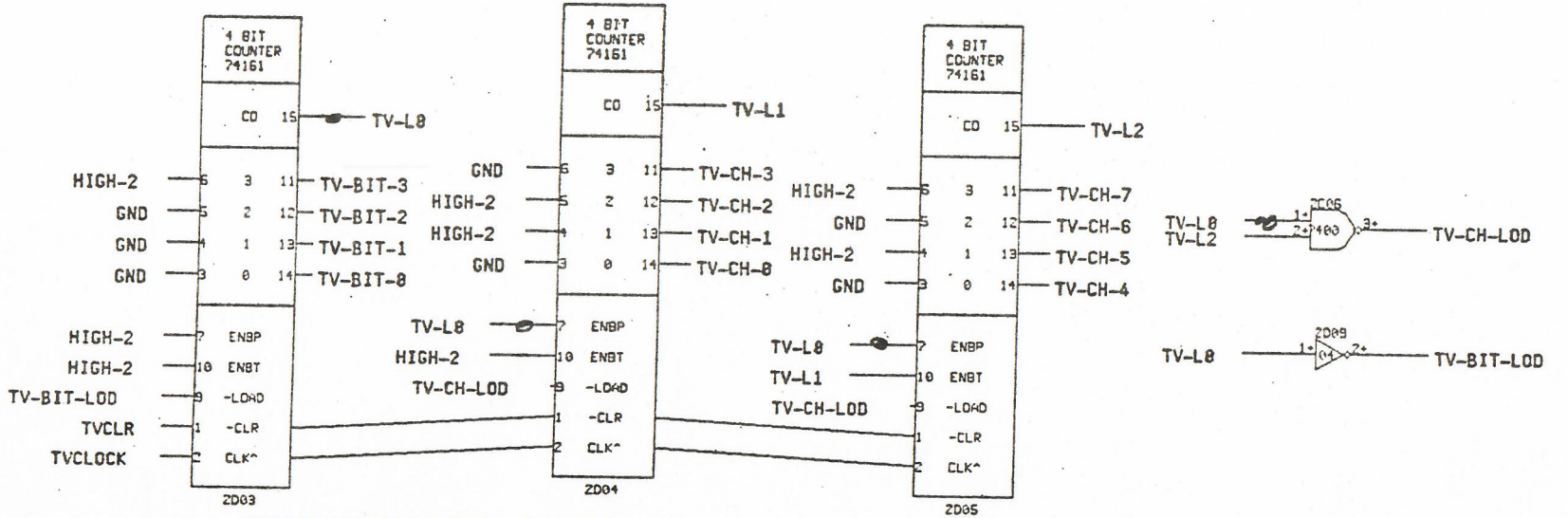
;1A10

;PINS 9 10 15 16 HAVE DAC PROTECTION DIODES

; PUT NEAR VECTOR GENERATOR



A-L-U CHIPS | MINSKY 2500 | 29-FEB-76 13:29 | HQM: NTFH17



NTFH18 COUNTER-CHAINS SHOULD NOT HAVE ANY CLEAR INPUT

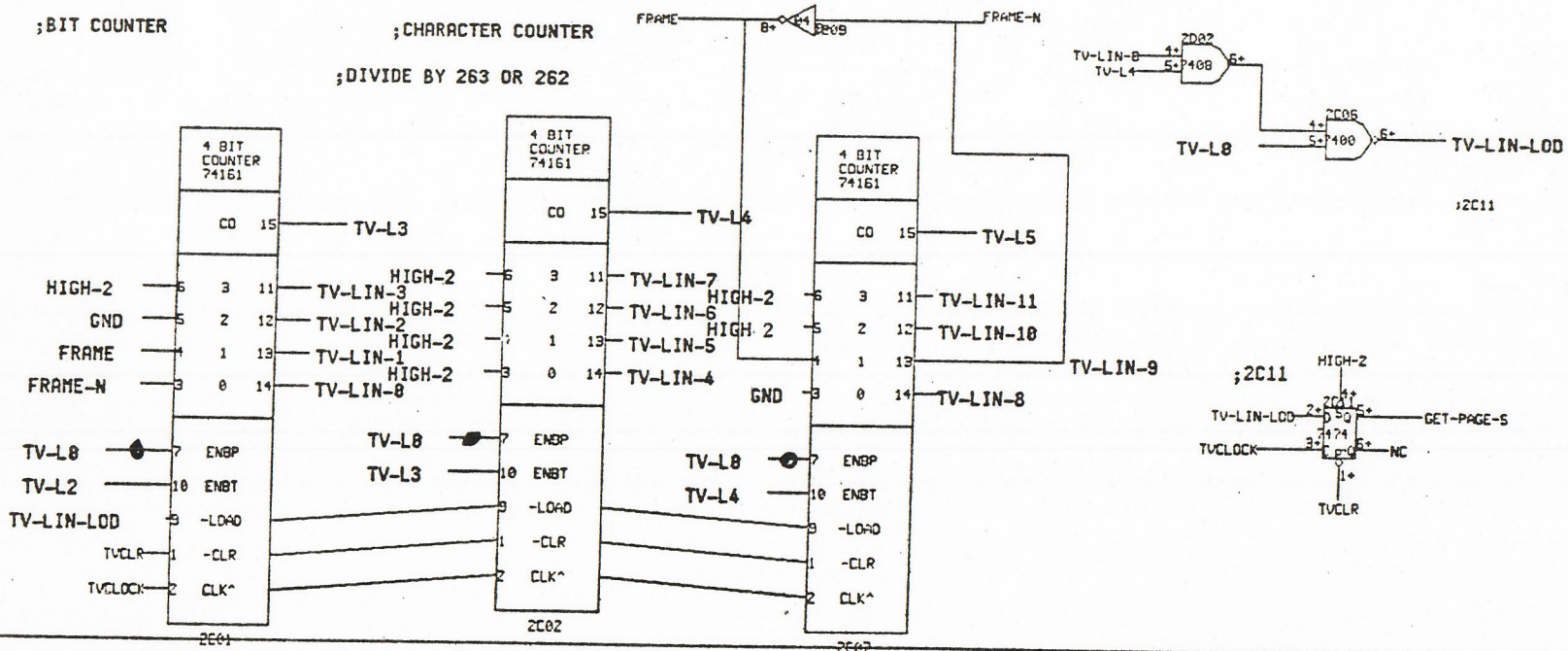
;DIVIDE BY 8

;BIT COUNTER

;DIVIDE BY 98

;CHARACTER COUNTER

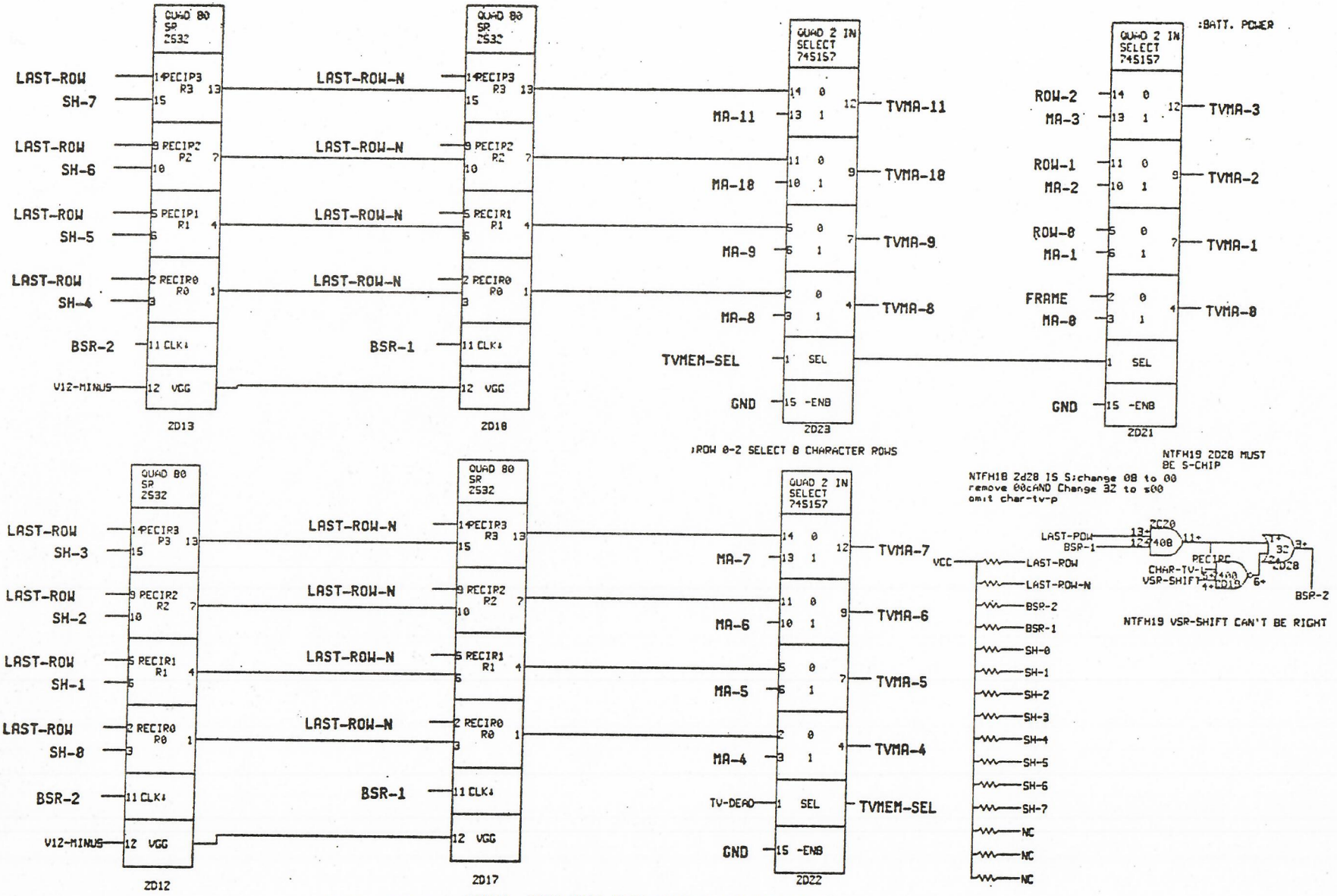
;DIVIDE BY 263 OR 262

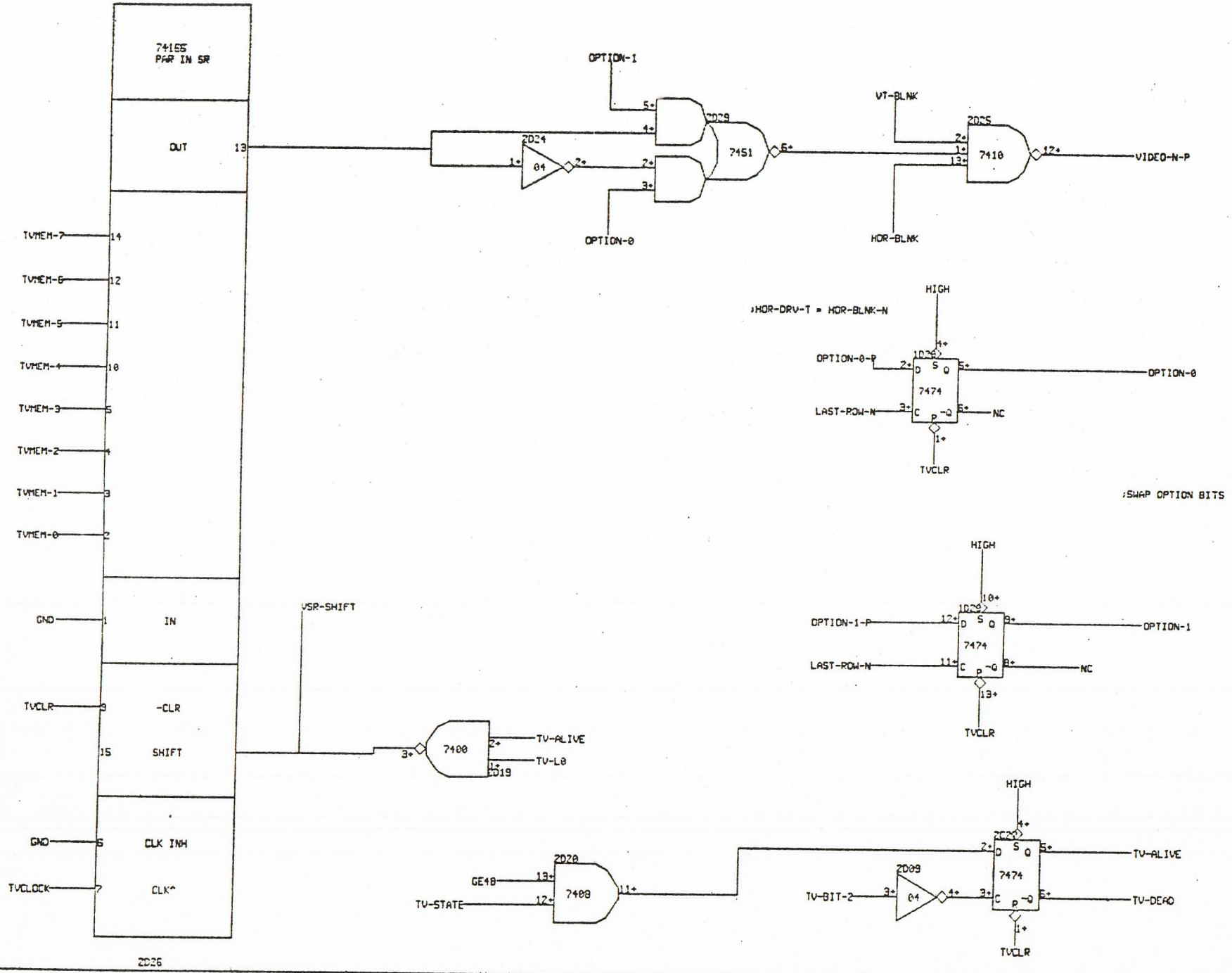


TIMING CHAIN

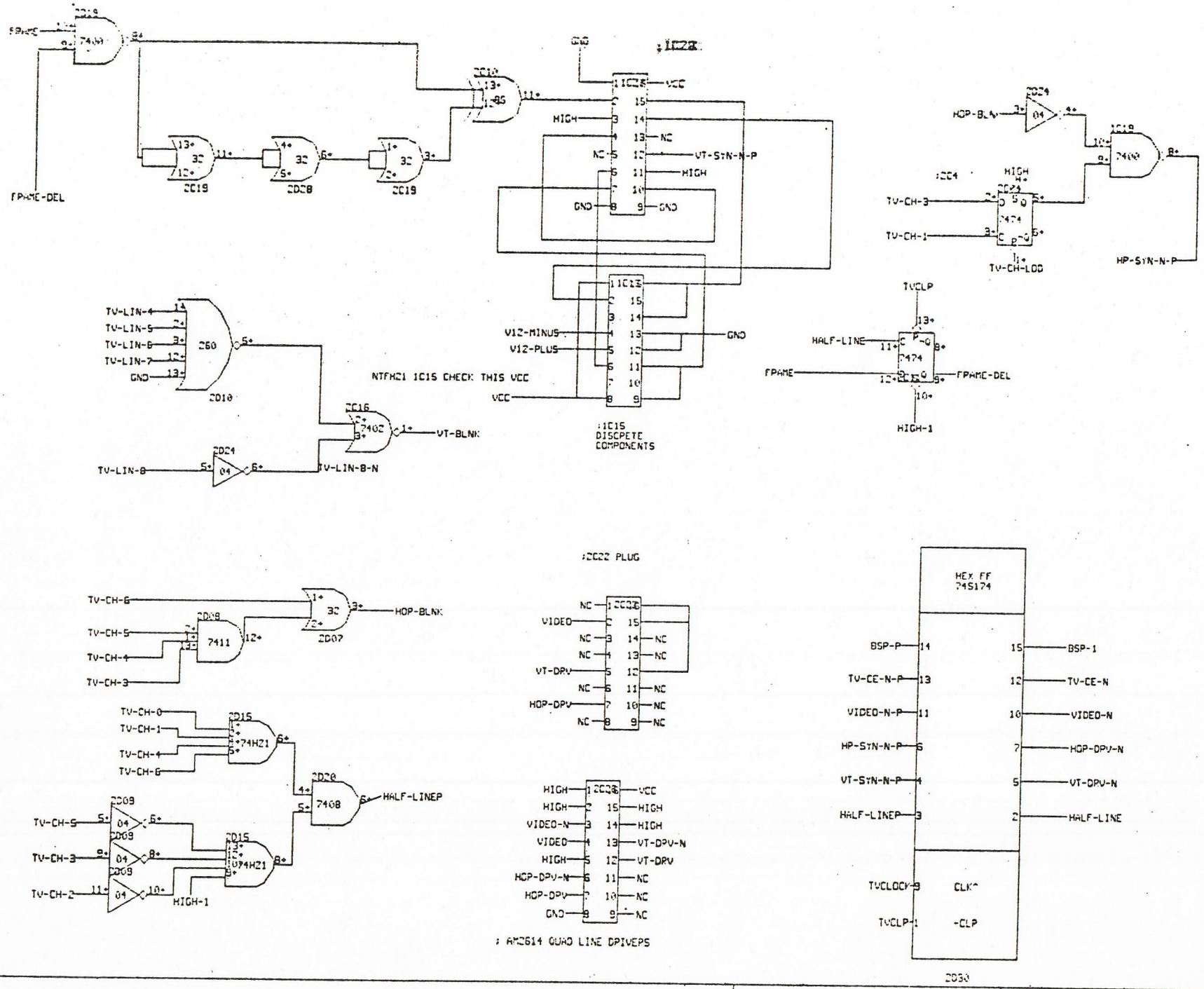
02-APR-76 15:14

HQM: NTFH18

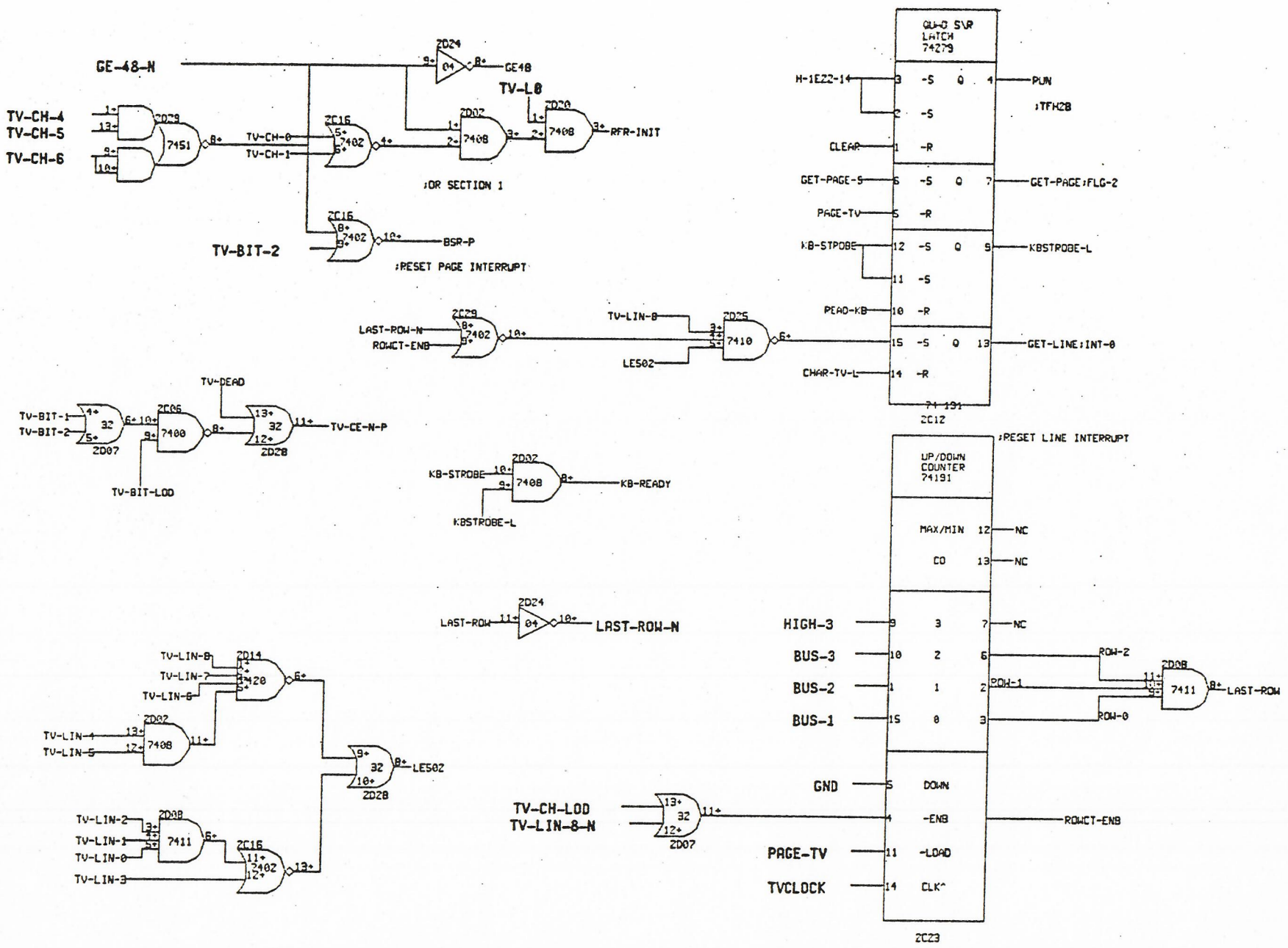

QUAD 80 SR 2532
ZD13
ZD18
LAST-ROW
SH-7
SH-6
SH-5
SH-4
BSR-2
V12-MINUS
LAST-ROW-N
BSR-1
QUAD 2 IN SELECT 74S157
ZD23
MA-11
MA-10
MA-9
MA-8
TVMEM-SEL
GND
TVMA-11
TVMA-10
TVMA-9
TVMA-8
;ROW 0-2 SELECT 8 CHARACTER ROWS
;BATT. POWER
ZD21
ROW-2
MA-3
ROW-1
MA-2
ROW-0
MA-1
FRAME
MA-0
TVMA-3
TVMA-2
TVMA-1
TVMA-0
SEL
-ENB
NTFH19 2D28 MUST BE S-CHIP
NTFH18 2d28 IS S;change 08 to 00
remove 00cAND Change 32 to s00
omit char-tv-p
ZC20
LAST-POW
BSR-1
PECIRC
CHAR-TV-P
VSR-SHIFT
2D28
BSR-2
NTFH19 VSR-SHIFT CAN'T BE RIGHT
VCC
LAST-ROW
LAST-ROW-N
BSR-2
BSR-1
SH-0
SH-1
SH-2
SH-3
SH-4
SH-5
SH-6
SH-7
NC
ZD12
ZD17
ZD22
TV-DEAD
TVMEM-SEL
MA-7
MA-6
MA-5
MA-4
TVMA-7
TVMA-6
TVMA-5
TVMA-4
;RECIRCULATE TEXT-LINE
TEXT-LINE
ZD23 MUST BE LS 157 CHIPS



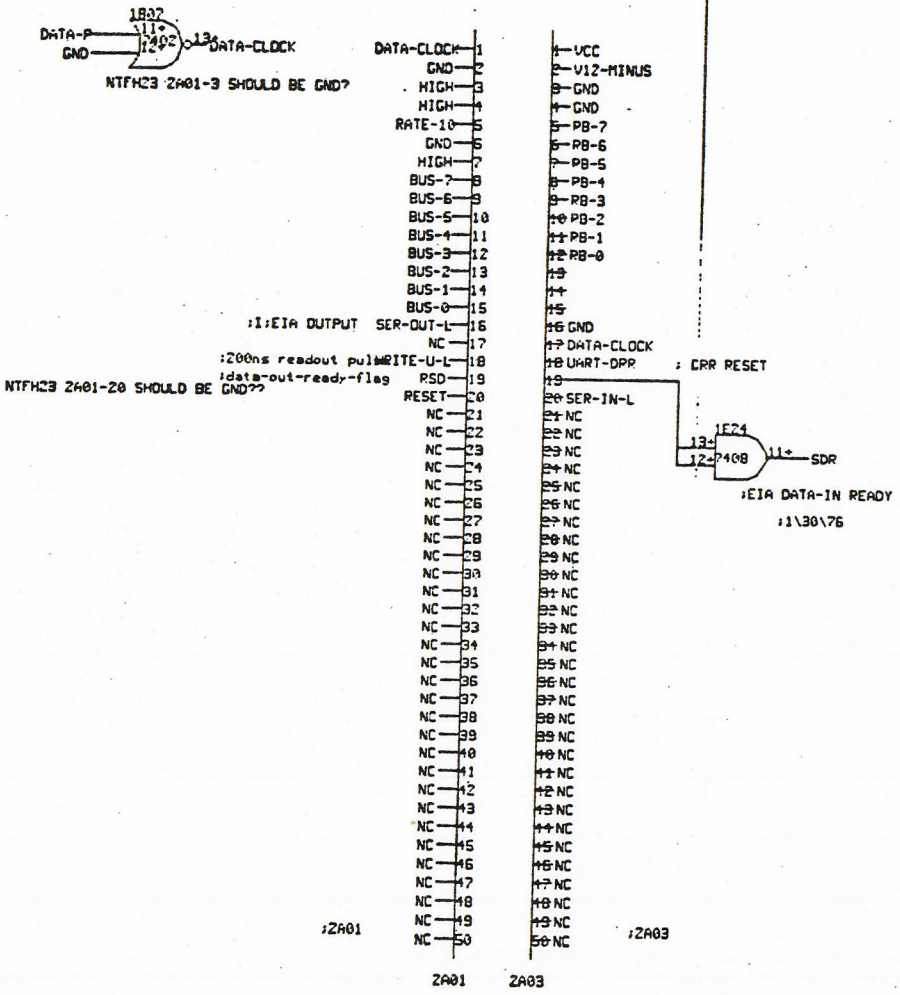
TV SIGNALS	INCLUDING DRIVERS	Ø2-APR-76 15:Ø9	HQM: NTFH2Ø

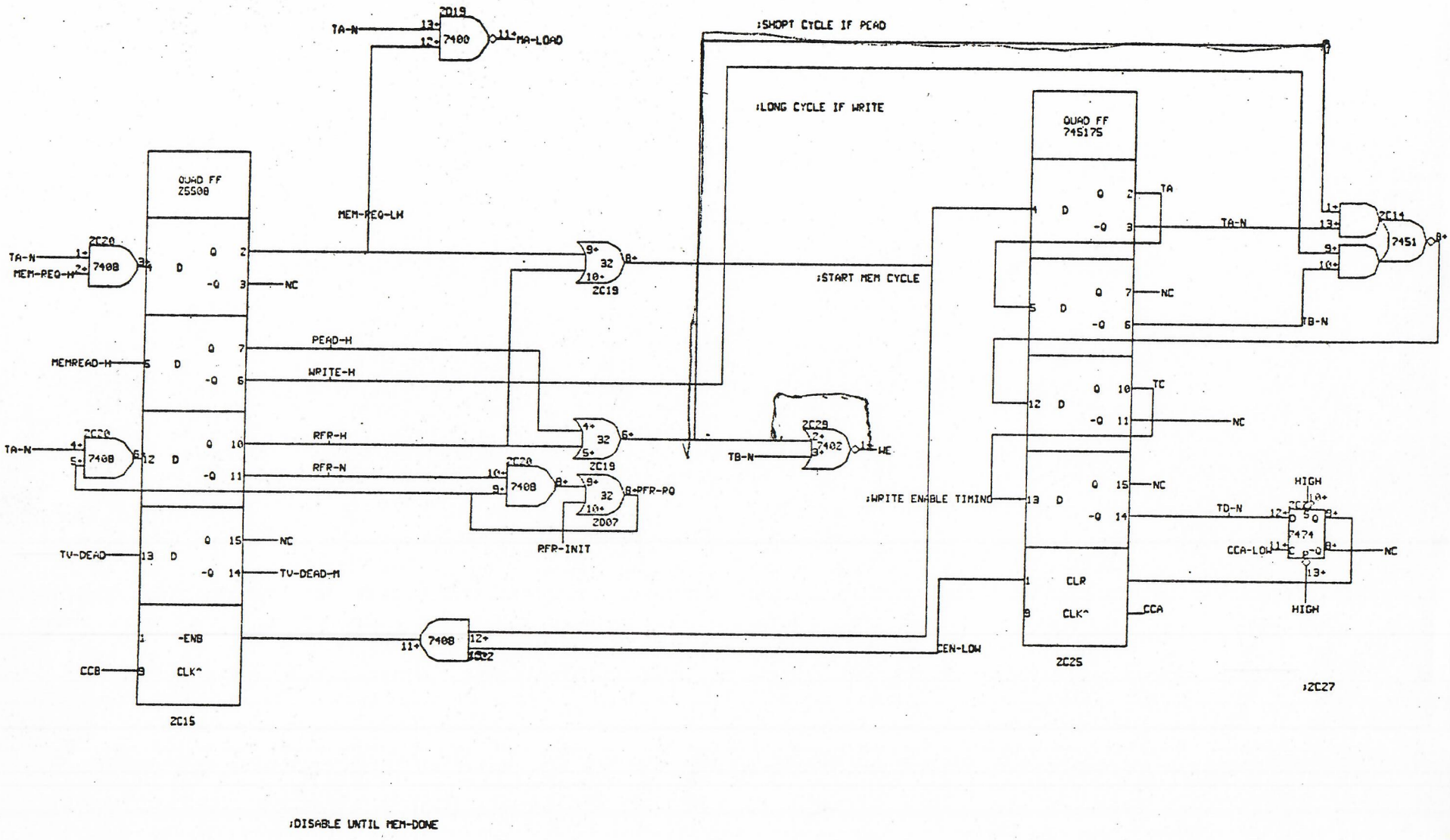


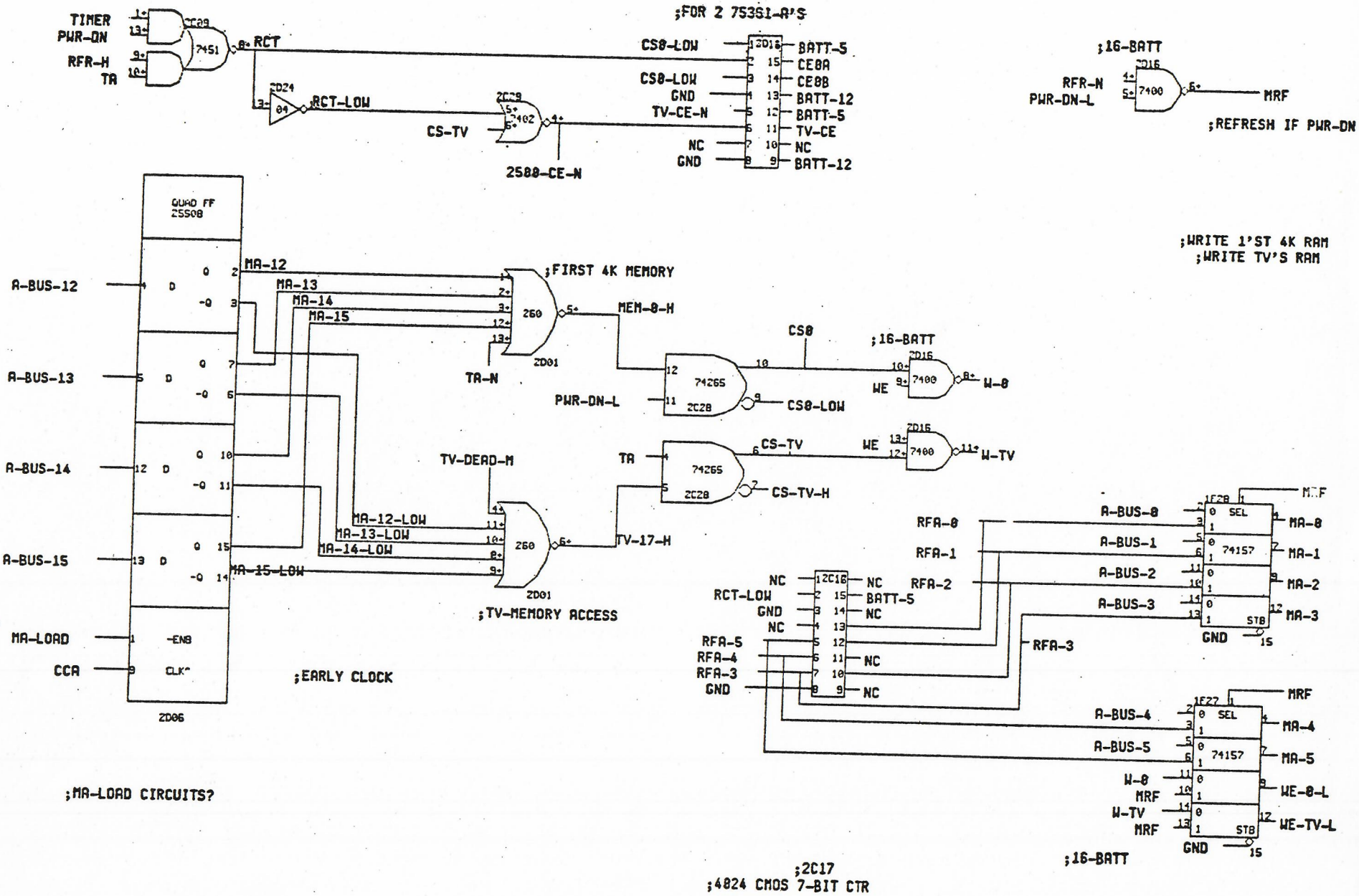
LINE BUFFERS | ADDRESS MULTIPLEXERS | Ø4-APR-76 22:18 | HQM: NTFH21



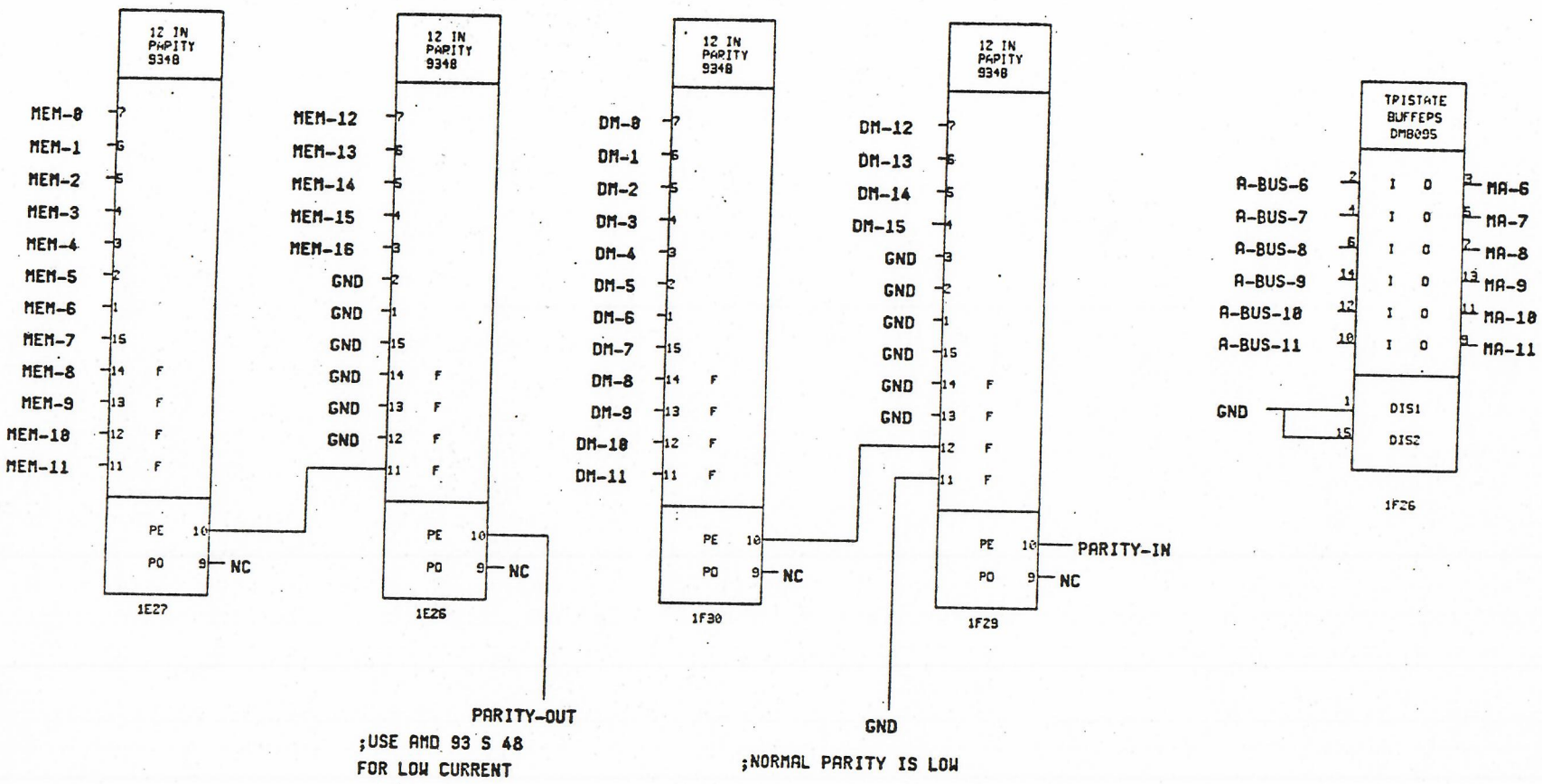
TV SIGNALS	INCLUDING DRIVERS	Ø2-APR-76 11:23	HQM: NTFH22

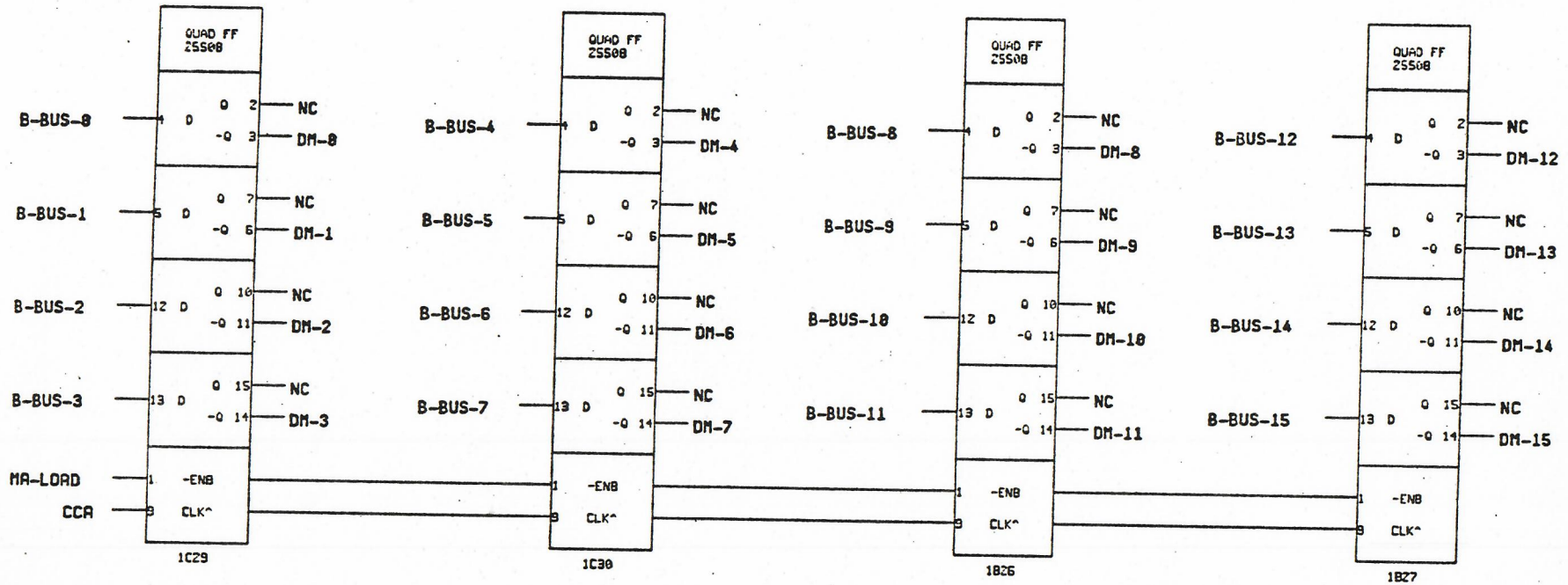

1B02
DATA-P
GND
DATA-CLOCK
NTFH23 ZA01-3 SHOULD BE GND?
;I;EIA OUTPUT
;200ns readout pulse
;data-out-ready-flag
NTFH23 ZA01-20 SHOULD BE GND??
WRITE-U-L
RSD
RESET
DATA-CLOCK
GND
HIGH
HIGH
RATE-10
GND
HIGH
BUS-7
BUS-6
BUS-5
BUS-4
BUS-3
BUS-2
BUS-1
BUS-0
SER-OUT-L
NC
;ZA01
VCC
V12-MINUS
GND
GND
PB-7
PB-6
PB-5
PB-4
PB-3
PB-2
PB-1
PB-0
GND
DATA-CLOCK
UART-DPR
; CRR RESET
SER-IN-L
;ZA03
1E24
2408
SDR
;EIA DATA-IN READY
;1\30\76
ZA01
ZA03

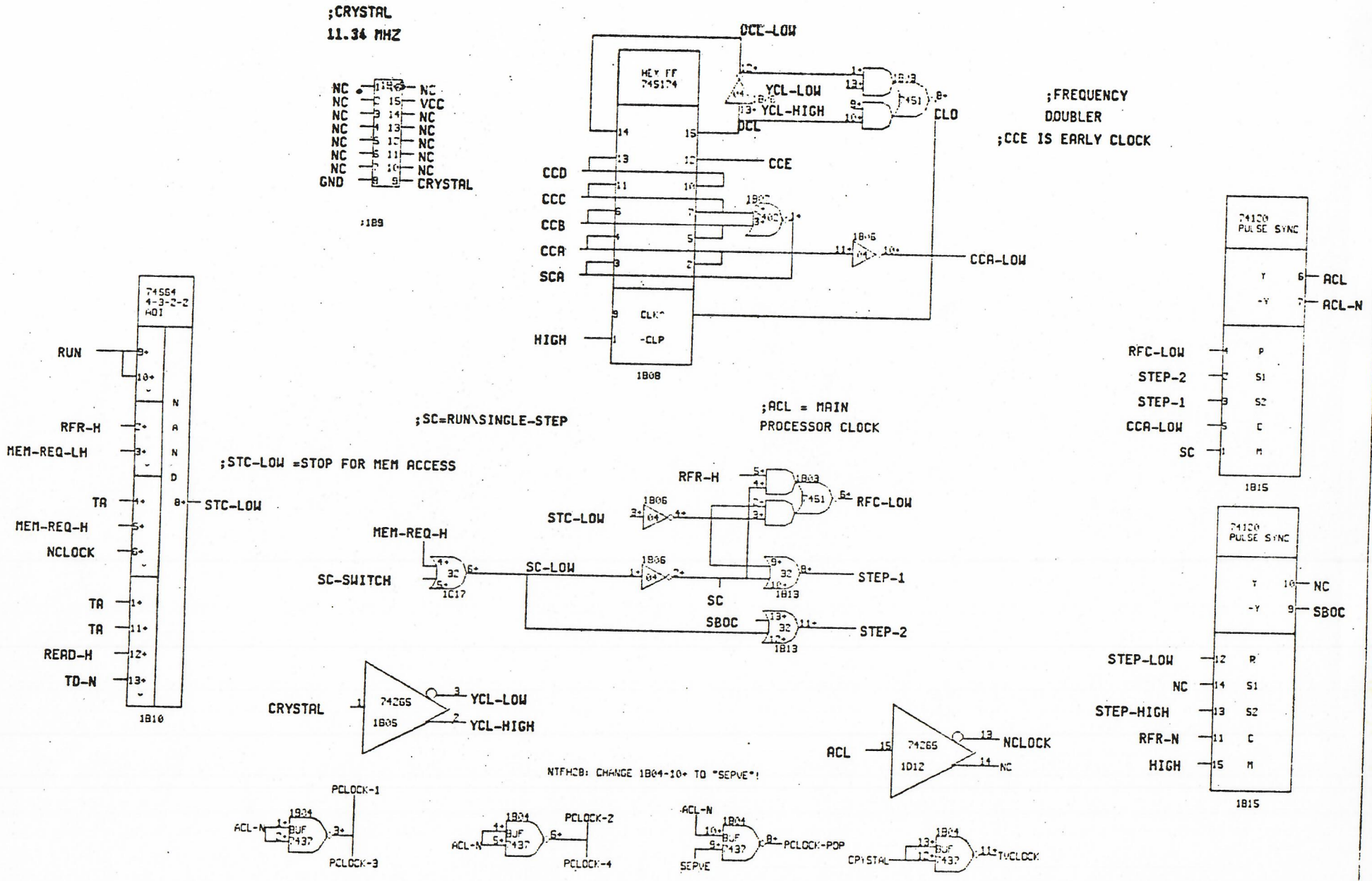

2D19
TA-N
7400
MA-LOAD
;SHORT CYCLE IF READ
;LONG CYCLE IF WRITE
QUAD FF
Z5508
MEM-REQ-LH
2C20
TA-N
MEM-REQ-H
7408
D
Q
-Q
NC
2C19
32
;START MEM CYCLE
QUAD FF
74S175
TA
TA-N
2C14
7451
TB-N
MEMREAD-H
READ-H
WRITE-H
RFR-H
RFR-N
2C29
7402
WE
TB-N
TC
;WRITE ENABLE TIMING
HIGH
TD-N
7474
CCA-LOW
RFR-PQ
2D07
RFR-INIT
TV-DEAD
TV-DEAD-M
-ENB
CLK^
CCB
2C15
CLR
CCA
CEN-LOW
2C25
;2C27
;DISABLE UNTIL MEM-DONE



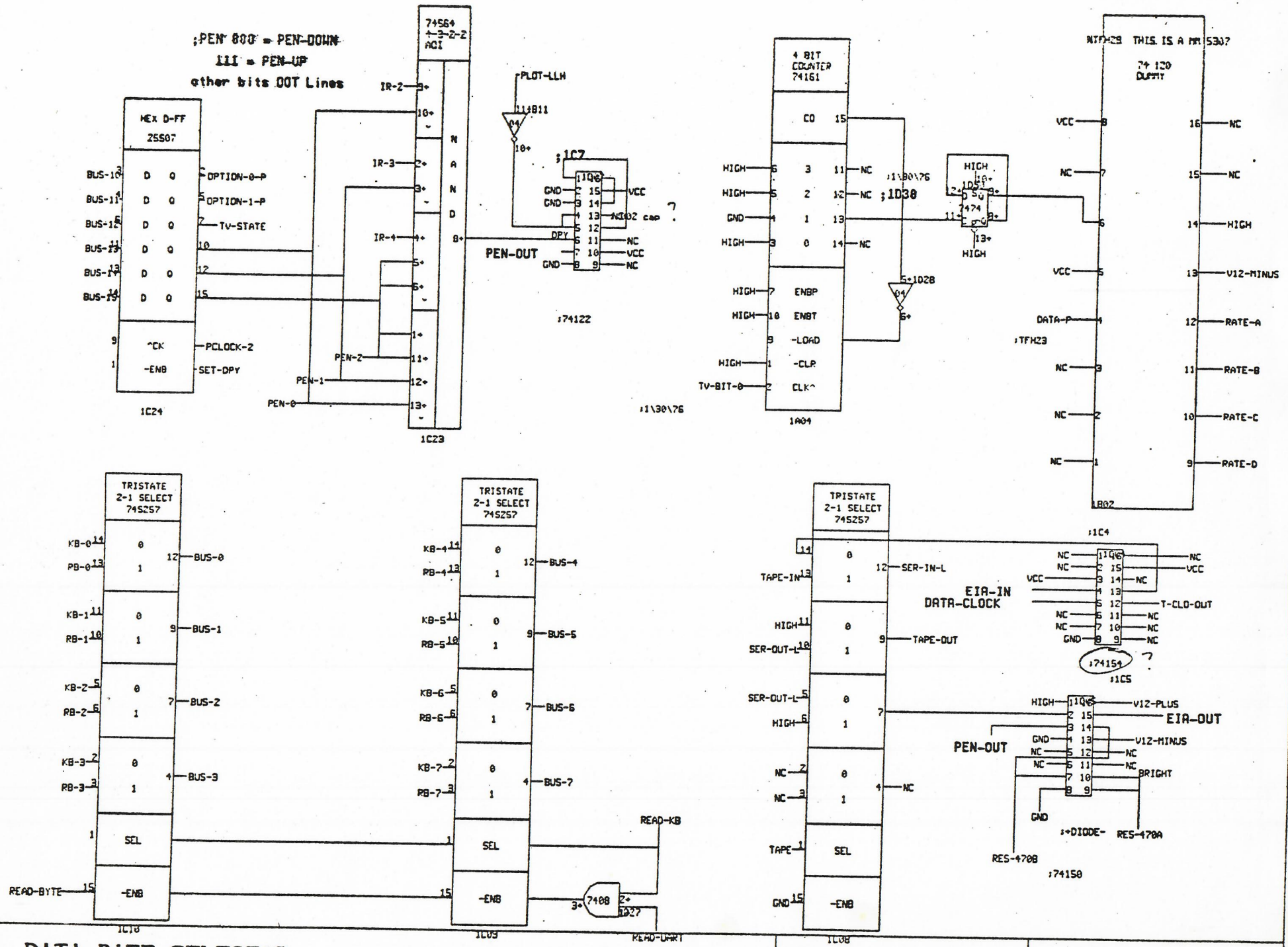
MEMORY ADDRESS REGISTER	2500	29-FEB-76 14:32	HQM: NTFH25


12 IN PARITY 9348
MEM-0
MEM-1
MEM-2
MEM-3
MEM-4
MEM-5
MEM-6
MEM-7
MEM-8
MEM-9
MEM-10
MEM-11
PE
PO
NC
1E27
MEM-12
MEM-13
MEM-14
MEM-15
MEM-16
GND
1E26
PARITY-OUT
;USE AMD 93 S 48
FOR LOW CURRENT
DM-0
DM-1
DM-2
DM-3
DM-4
DM-5
DM-6
DM-7
DM-8
DM-9
DM-10
DM-11
1F30
DM-12
DM-13
DM-14
DM-15
1F29
PARITY-IN
GND
;NORMAL PARITY IS LOW
TRISTATE BUFFERS DM8095
A-BUS-6
A-BUS-7
A-BUS-8
A-BUS-9
A-BUS-10
A-BUS-11
MA-6
MA-7
MA-8
MA-9
MA-10
MA-11
DIS1
DIS2
1F26


QUAD FF
25S08
B-BUS-0
B-BUS-1
B-BUS-2
B-BUS-3
MA-LOAD
CCA
NC
DM-0
DM-1
DM-2
DM-3
-ENB
CLK^
1C29
B-BUS-4
B-BUS-5
B-BUS-6
B-BUS-7
DM-4
DM-5
DM-6
DM-7
1C30
B-BUS-8
B-BUS-9
B-BUS-10
B-BUS-11
DM-8
DM-9
DM-10
DM-11
1B26
B-BUS-12
B-BUS-13
B-BUS-14
B-BUS-15
DM-12
DM-13
DM-14
DM-15
1B27



CLOCK CONTROL	2500	04-APR-76 22:57	HQM: NTFH28

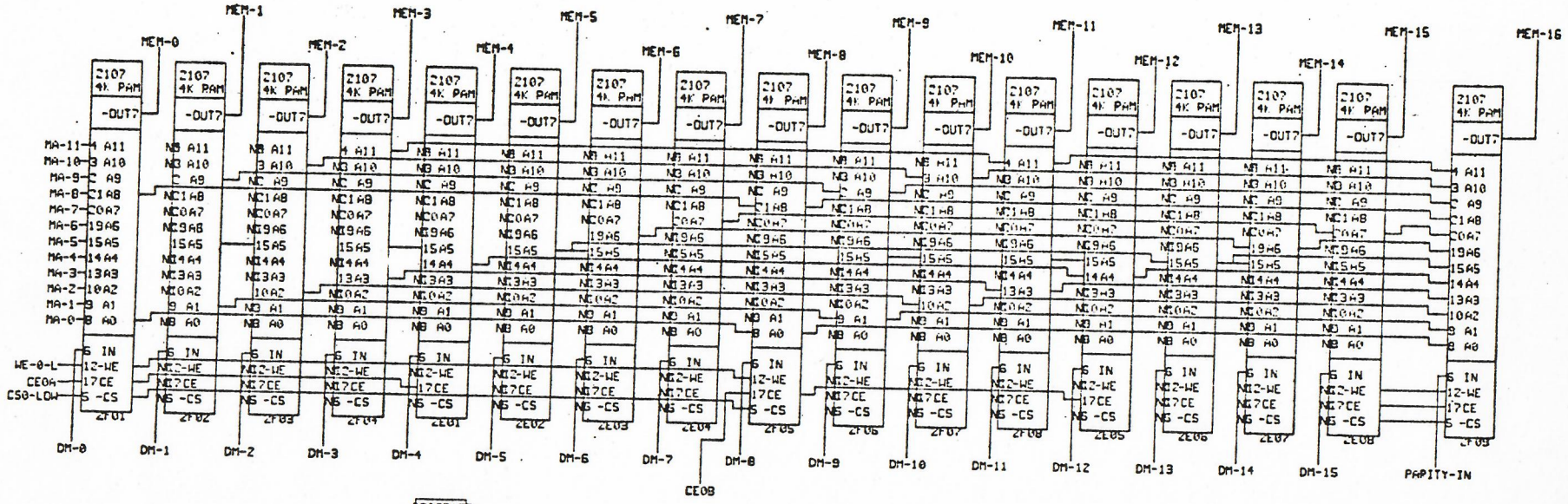


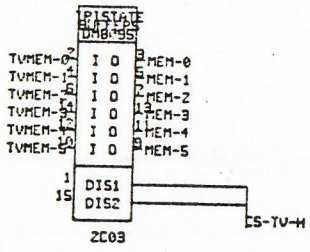
DATA RATE SELECTOR

31-MAR-76 16:27

HQM: NTFH29

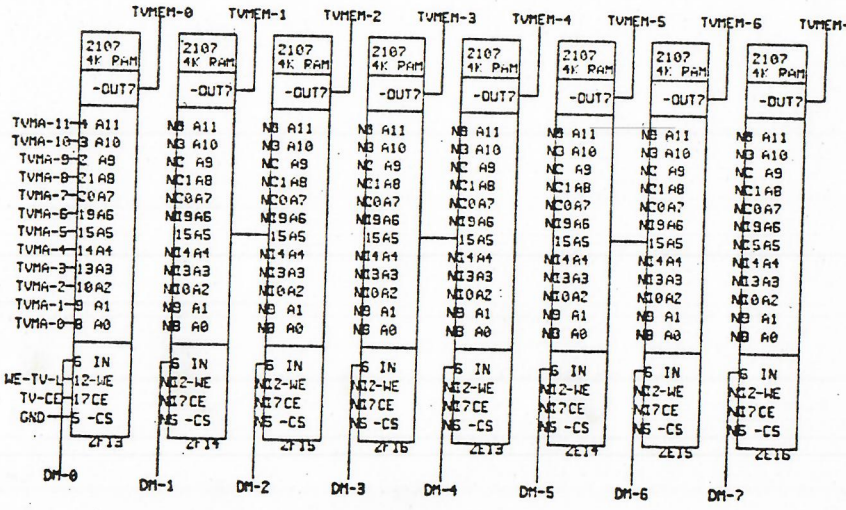
;FIRST 4K OF MAIN MEMORY on main board





;other two gates on
1C14 (TFH-10)

CONNECT
2E13-1 2EJ1-3 (BATT-5-N)
2E16-1 2EJ1-4
2E13-18 2EJ1-11 (BATT-12)
2E16-18 2EJ1-12
2E13-11 2EJ1-05 (BATT-5)
2E16-11 2EJ1-06
BE SURE WIRELIST DOESN'T CONNECT 1-18-11 ON MEMORY CHIPS



;use signetics 2604's

;4K BY 8-BIT FONT MEMORY